Pallab Dasgupta

List of Publications by Citations

70 papers	229 citations	7 h-index	10 g-index
92 ext. papers	315 ext. citations	1.9 avg, IF	3.22 L-index

#	Paper	IF	Citations
70	Policy Based Security Analysis in Enterprise Networks: A Formal Approach. *IEEE Transactions on Network and Service Management*, **2010**, 7, 231-243	4.8	20
69	Instrumenting AMS assertion verification on commercial platforms. *ACM Transactions on Design Automation of Electronic Systems*, **2009**, 14, 1-47	1.5	19
68	Feature Indented Assertions for Analog and Mixed-Signal Validation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1928-1941	2.5	12
67	Leveraging UPF-extracted assertions for modeling and formal verification of architectural power intent **2010**,		11
66	Auxiliary Specifications for Context-Sensitive Monitoring of AMS Assertions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 1446-1457	2.5	9
65	Automatic Characterization of Exploitable Faults: A Machine Learning Approach. *IEEE Transactions on Information Forensics and Security*, **2019**, 14, 954-968	8	9
64	POWER-TRUCTOR: An Integrated Tool Flow for Formal Verification and Coverage of Architectural Power Intent. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1801-1813	2.5	8
63	Formal Verification of Hardware / Software Power Management Strategies **2013**,		7
62	Synchronizing AMS Assertions with AMS Simulation. *ACM Transactions on Design Automation of Electronic Systems*, **2012**, 17, 1-25	1.5	7
61	Accelerating Assertion Coverage With Adaptive Testbenches. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2008**, 27, 967-972	2.5	7
60	Satisfiability Models for Maximum Transition Power. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2008**, 16, 941-951	2.6	7
59	Computing Minimal Debugging Windows in Failure Traces of AMS Assertions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1776-1781	2.5	6
58	Breaking Redundancy-Based Countermeasures with Random Faults and Power Side Channel **2018**,		6
57	Counterexample Ranking Using Mined Invariants. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 1978-1991	2.5	5
56	Formal Hardware/Software Co-Verification of Embedded Power Controllers. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2014**, 33, 2025-2029	2.5	5
55	Incorporating local variables in mixed-signal assertions **2009**,		5
54	Formal Methods for Early Analysis of Functional Reliability in Component-Based Embedded Applications. *IEEE Embedded Systems Letters*, **2013**, 5, 8-11	1	4

53	Formal Interpretation of Assertion-Based Features on AMS Designs. *IEEE Design and Test*, **2014**, 1-1	1.4	4
52	Assertion Aware Sampling Refinement: A Mixed-Signal Perspective. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 1772-1776	2.5	4
51	Cohesive Coverage Management for Simulation and Formal Property Verification **2008**,		4
50	Formal Methods for Pattern Based Reliability Analysis in Embedded Systems **2015**,		3
49	Formal Feature Interpretation of Hybrid Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2474-2484	2.5	3
48	Formal Methods for Validation and Test Point Prioritization in Railway Signaling Logic. *IEEE Transactions on Intelligent Transportation Systems*, **2017**, 18, 678-689	6.1	3
47	Route optimization for an electric vehicle with priority destinations **2017**,		3
46	Synthesis of sampling modes for adaptive control **2014**,		3
45	A Verification framework for Analyzing Security Implementations in an Enterprise LAN **2009**,		3
44	Bounded Delay Timing Analysis Using Boolean Satisfiability **2007**,		3
43	Interpreting Local Variables in AMS Assertions During Simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 980-984	2.5	3
42	Hierarchical Program-Triggered Reinforcement Learning Agents for Automated Driving. *IEEE Transactions on Intelligent Transportation Systems*, **2021**, 1-10	6.1	3
41	An automated framework for exploitable fault identification in block ciphers. *Journal of Cryptographic Engineering*, **2019**, 9, 203-219	1.9	2
40	Algorithmic approaches for optimizing electronic control unit time using multi-rate sampling. *Control Theory and Technology*, **2018**, 16, 173-190	1	2
39	Co-Synthesis of Loop Execution Patterns for Multihop Control Networks. *IEEE Embedded Systems Letters*, **2018**, 10, 111-114	1	2
38	Auxiliary State Machines and Auxiliary Functions: Constructs for Extending AMS Assertions **2011**,		2
37	Fault Analysis of Security Policy Implementations in Enterprise Networks **2009**,		2
36	Formal methods for ranking counterexamples through assumption mining **2012**,		2

35	Inline Assertions - Embedding Formal Properties in a Test Bench **2009**,		2
34	SAT based solutions for consistency problems in formal property specifications for open systems		2
33	Performance and energy aware robust specification of control execution patterns under dropped samples. *IET Computers and Digital Techniques*, **2019**, 13, 493-504	0.9	2
32	Feature Based Coverage Analysis of AMS Circuits **2018**,		2
31	Solar Irradiance Prediction from Historical Trends Using Deep Neural Networks **2018**,		2
30	Generating AMS Behavioral Models with Formal Guarantees on Feature Accuracy **2017**,		1
29	ForFET: A Formal Feature Evaluation Tool for Hybrid Systems. *Lecture Notes in Computer Science*, **2017**, 437-445	0.9	1
28	Monitoring AMS Simulation: From Assertions to Features **2015**,		1
27	Assertions for Protecting Mixed-Signal Latency Contracts in Power Management. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1745-1756	2.6	1
26	Synthesizing Performance-Aware (m, k)-Firm Control Execution Patterns Under Dropped Samples **2019**,		1
25	Early Analysis of Critical Faults: An Approach to Test Generation From Formal Specifications. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2012**, 31, 447-451	2.5	1
24	Adaptive sharing of sampling rates among software based controllers **2015**,		1
23	Acceptance and random generation of event sequences under real time calculus constraints **2014**,		1
22	Cohesive Coverage Management: Simulation Meets Formal Methods. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2012**, 28, 449-468	0.7	1
21	A Generalized Theory for Formal Assertion Coverage **2012**,		1
20	Coverage Management with Inline Assertions and Formal Test Points **2010**,		1
19	An end to end correctness verification approach for application specific usage control **2009**,		1
18	The BUSpec platform for automated generation of verification aids for standard bus protocols **2004**,		1

List of Publications

17	A Branching Time Temporal Framework for Quantitative Reasoning. *Journal of Automated Reasoning*, **2003**, 30, 205-232	1	1
16	Recurrence in Dense-time AMS Assertions. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 1-1	2.5	1
15	A Structured Approach for Rapid Identification of Fault-Sensitive Nets in Analog Circuits **2019**,		1
14	A Methodology for Identification of Internal Nets for Improving Fault Coverage in Analog and Mixed Signal Circuits. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **2020**, 36, 719-730	0.7	0
13	Reliability Guarantees in Automata-Based Scheduling for Embedded Control Software. *IEEE Embedded Systems Letters*, **2013**, 5, 17-20	1	0
12	Pattern Guided Integrated Scheduling and Routing in Multi-Hop Control Networks. *Transactions on Embedded Computing Systems*, **2020**, 19, 1-28	1.8	0
11	SongF0: A Spectrum-Based Fundamental Frequency Estimation for Monophonic Songs. *Circuits, Systems, and Signal Processing*, **2021**, 40, 772-797	2.2	0
10	SMT-Based Verification of Safety-Critical Embedded Control Software. *IEEE Embedded Systems Letters*, **2021**, 13, 138-141	1	0
9	Min-max event-triggered computation tree logic. *Sadhana - Academy Proceedings in Engineering Sciences*, **2002**, 27, 163-180	1	
8	Heuristic search strategies for multiobjective state space search. *Sadhana - Academy Proceedings in Engineering Sciences*, **1996**, 21, 263-290	1	
7	ExpFault: An Automated Framework for Block Cipher Fault Analysis **2019**, 13-57		
6	Exploitable Fault Space Characterization: A Complementary Approach **2019**, 59-88		
5	(hf_0): A Hybrid Pitch Extraction Method for Multimodal Voice. *Circuits, Systems, and Signal Processing*, **2021**, 40, 262-275	2.2	
4	Usage-Driven Personalization of Power Management Logic. *IEEE Embedded Systems Letters*, **2021**, 13, 106-109	1	
3	Performance-Driven Post-Processing of Control Loop Execution Schedules. *ACM Transactions on Design Automation of Electronic Systems*, **2021**, 26, 1-27	1.5	
2	Migrating Assertions from Dense to Discrete Time. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	
1	Safe and Stable RL (S2RL) Driving Policies Using Control Barrier and Control Lyapunov Functions. *IEEE Transactions on Intelligent Vehicles*, **2022**, 1-1	5	