List of Publications by Year in descending order

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DALLAR DASCUDTA

| #  | Article  | IF  | CITATIONS |
|----|--|-----|-----------|
| 1  | Policy Based Security Analysis in Enterprise Networks: A Formal Approach. IEEE Transactions on<br>Network and Service Management, 2010, 7, 231-243.  | 3.2 | 27        |
| 2  | Instrumenting AMS assertion verification on commercial platforms. ACM Transactions on Design<br>Automation of Electronic Systems, 2009, 14, 1-47.  | 1.9 | 25        |
| 3  | Feature Indented Assertions for Analog and Mixed-Signal Validation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1928-1941.  | 1.9 | 18        |
| 4  | Automatic Characterization of Exploitable Faults: A Machine Learning Approach. IEEE Transactions on<br>Information Forensics and Security, 2019, 14, 954-968.  | 4.5 | 18        |
| 5  | Hierarchical Program-Triggered Reinforcement Learning Agents for Automated Driving. IEEE<br>Transactions on Intelligent Transportation Systems, 2022, 23, 10902-10911.   | 4.7 | 16        |
| 6  | Leveraging UPF-extracted assertions for modeling and formal verification of architectural power intent. , 2010, , .  |     | 15        |
| 7  | Auxiliary Specifications for Context-Sensitive Monitoring of AMS Assertions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1446-1457.                                     | 1.9 | 15        |
| 8  | POWER-TRUCTOR: An Integrated Tool Flow for Formal Verification and Coverage of Architectural<br>Power Intent. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32,<br>1801-1813. | 1.9 | 11        |
| 9  | Accelerating Assertion Coverage With Adaptive Testbenches. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 967-972.   | 1.9 | 10        |
| 10 | Breaking Redundancy-Based Countermeasures with Random Faults and Power Side Channel. , 2018, , .   |     | 10        |
| 11 | Synchronizing AMS Assertions with AMS Simulation. ACM Transactions on Design Automation of Electronic Systems, 2012, 17, 1-25.   | 1.9 | 9         |
| 12 | Formal Verification of Hardware / Software Power Management Strategies. , 2013, , .  |     | 8         |
| 13 | Satisfiability Models for Maximum Transition Power. IEEE Transactions on Very Large Scale<br>Integration (VLSI) Systems, 2008, 16, 941-951.  | 2.1 | 7         |
| 14 | Formal Interpretation of Assertion Based Features on AMS Designs. IEEE Design and Test, 2014, , 1-1.   | 1.1 | 7         |
| 15 | Formal Methods for Validation and Test Point Prioritization in Railway Signaling Logic. IEEE<br>Transactions on Intelligent Transportation Systems, 2017, 18, 678-689.   | 4.7 | 7         |
| 16 | Solar Irradiance Prediction from Historical Trends Using Deep Neural Networks. , 2018, , .   |     | 7         |
| 17 | A Structured Approach for Rapid Identification of Fault-Sensitive Nets in Analog Circuits. , 2019, , .   |     | 7         |
| 18 | Formal methods for analyzing the completeness of an assertion suite against a high-level fault model. , 0, , .   |     | 6         |

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|----|--|-----|-----------|
| 19 | Incorporating local variables in mixed-signal assertions. , 2009, , .  |     | 6         |
| 20 | Computing Minimal Debugging Windows in Failure Traces of AMS Assertions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1776-1781. | 1.9 | 6         |
| 21 | Formal Methods for Early Analysis of Functional Reliability in Component-Based Embedded<br>Applications. IEEE Embedded Systems Letters, 2013, 5, 8-11.                       | 1.3 | 6         |
| 22 | Counterexample Ranking Using Mined Invariants. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1978-1991.                           | 1.9 | 6         |
| 23 | Formal Hardware/Software Co-Verification of Embedded Power Controllers. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 2025-2029.  | 1.9 | 6         |
| 24 | Synthesis of sampling modes for adaptive control. , 2014, , .  |     | 6         |
| 25 | Cohesive Coverage Management for Simulation and Formal Property Verification. , 2008, , .  |     | 5         |
| 26 | Fault Analysis of Security Policy Implementations in Enterprise Networks. , 2009, , .  |     | 5         |
| 27 | Auxiliary State Machines and Auxiliary Functions: Constructs for Extending AMS Assertions. , 2011, , .   |     | 5         |
| 28 | The BUSpec platform for automated generation of verification aids for standard bus protocols. , 2004, , .  |     | 4         |
| 29 | Bounded Delay Timing Analysis Using Boolean Satisfiability. , 2007, , .  |     | 4         |
| 30 | An end to end correctness verification approach for application specific usage control. , 2009, , .  |     | 4         |
| 31 | A Verification framework for Analyzing Security Implementations in an Enterprise LAN. , 2009, , .  |     | 4         |
| 32 | Assertion Aware Sampling Refinement: A Mixed-Signal Perspective. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1772-1776.         | 1.9 | 4         |
| 33 | Reliability Guarantees in Automata-Based Scheduling for Embedded Control Software. IEEE Embedded<br>Systems Letters, 2013, 5, 17-20.   | 1.3 | 4         |
| 34 | Adaptive sharing of sampling rates among software based controllers. , 2015, , .   |     | 4         |
| 35 | Route optimization for an electric vehicle with priority destinations. , 2017, , .   |     | 4         |
| 36 | An automated framework for exploitable fault identification in block ciphers. Journal of Cryptographic Engineering, 2019, 9, 203-219.  | 1.5 | 4         |

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|----|--|-----|-----------|
| 37 | CoveRT: A Coverage Reporting Tool for Analog Mixed-Signal Designs. , 2020, , .   |     | 4         |
| 38 | Safe and Stable RL (S <sup>2</sup> RL) Driving Policies Using Control Barrier and Control Lyapunov<br>Functions. IEEE Transactions on Intelligent Vehicles, 2023, 8, 1889-1899.                    | 9.4 | 4         |
| 39 | SAT based solutions for consistency problems in formal property specifications for open systems. , 0, ,  |     | 3         |
| 40 | Formal Methods for Pattern Based Reliability Analysis in Embedded Systems. , 2015, , .   |     | 3         |
| 41 | Algorithmic approaches for optimizing electronic control unit time using multi-rate sampling.<br>Control Theory and Technology, 2018, 16, 173-190.   | 1.0 | 3         |
| 42 | Formal Feature Interpretation of Hybrid Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2474-2484.   | 1.9 | 3         |
| 43 | Co-Synthesis of Loop Execution Patterns for Multihop Control Networks. IEEE Embedded Systems<br>Letters, 2018, 10, 111-114.  | 1.3 | 3         |
| 44 | Interpreting Local Variables in AMS Assertions During Simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 980-984.                                | 1.9 | 3         |
| 45 | Recurrence in Dense-Time AMS Assertions. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2416-2420.   | 1.9 | 3         |
| 46 | SongFO: A Spectrum-Based Fundamental Frequency Estimation for Monophonic Songs. Circuits,<br>Systems, and Signal Processing, 2021, 40, 772-797.  | 1.2 | 3         |
| 47 | A formal approach for specification-driven AMS behavioral model generation. , 2009, , .  |     | 2         |
| 48 | Inline Assertions - Embedding Formal Properties in a Test Bench. , 2009, , .   |     | 2         |
| 49 | Formal methods for ranking counterexamples through assumption mining. , 2012, , .  |     | 2         |
| 50 | Cohesive Coverage Management: Simulation Meets Formal Methods. Journal of Electronic Testing:<br>Theory and Applications (JETTA), 2012, 28, 449-468.   | 0.9 | 2         |
| 51 | Early Analysis of Critical Faults: An Approach to Test Generation From Formal Specifications. IEEE<br>Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 447-451. | 1.9 | 2         |
| 52 | Handling fault detection latencies in automata-based scheduling for embedded control software. , 2013, , .   |     | 2         |
| 53 | Feature Based Coverage Analysis of AMS Circuits. , 2018, , .   |     | 2         |
| 54 | Synthesizing Performance-Aware (m, k)-Firm Control Execution Patterns Under Dropped Samples. ,<br>2019, , .  |     | 2         |

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|----|---|-----|-----------|
| 55 | The Notion of Cross Coverage in AMS Design Verification. , 2020, , .  |     | 2         |
| 56 | Performance and energy aware robust specification of control execution patterns under dropped samples. IET Computers and Digital Techniques, 2019, 13, 493-504.   | 0.9 | 2         |
| 57 | Pattern Guided Integrated Scheduling and Routing in Multi-Hop Control Networks. Transactions on Embedded Computing Systems, 2020, 19, 1-28.   | 2.1 | 2         |
| 58 | A Branching Time Temporal Framework for Quantitative Reasoning. Journal of Automated Reasoning, 2003, 30, 205-232.  | 1.1 | 1         |
| 59 | Formal Verification of Power Scheduling Policies for Battery Powered Mobile Systems. , 2006, , .  |     | 1         |
| 60 | Timing Analysis of Sequential Circuits Using Symbolic Event Propagation. , 2007, , .  |     | 1         |
| 61 | Abstraction refinement for state space partitioning based on auxiliary state machines. , 2009, , .  |     | 1         |
| 62 | Coverage Management with Inline Assertions and Formal Test Points. , 2010, , .  |     | 1         |
| 63 | A Generalized Theory for Formal Assertion Coverage. , 2012, , .   |     | 1         |
| 64 | Acceptance and random generation of event sequences under real time calculus constraints. , 2014, , .   |     | 1         |
| 65 | Monitoring AMS Simulation: From Assertions to Features. , 2015, , .   |     | 1         |
| 66 | Generating AMS Behavioral Models with Formal Guarantees on Feature Accuracy. , 2017, , .  |     | 1         |
| 67 | Fault Vulnerability Ranking of Transistors in Analog Integrated Circuits using AC Analysis. , 2020, , .   |     | 1         |
| 68 | A Methodology for Identification of Internal Nets for Improving Fault Coverage in Analog and Mixed<br>Signal Circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 2020, 36, 719-730. | 0.9 | 1         |
| 69 | Assertions for Protecting Mixed-Signal Latency Contracts in Power Management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1745-1756.                                      | 2.1 | 1         |
| 70 | \$\$hf_0\$\$: A Hybrid Pitch Extraction Method for Multimodal Voice. Circuits, Systems, and Signal Processing, 2021, 40, 262-275.   | 1.2 | 1         |
| 71 | SMT-Based Verification of Safety-Critical Embedded Control Software. IEEE Embedded Systems Letters, 2021, 13, 138-141.  | 1.3 | 1         |
| 72 | Migrating Assertions From Dense to Discrete Time. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2362-2371.   | 1.9 | 1         |

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|----|---|-----|-----------|
| 73 | POWER-SIM: An SOC Simulator for Estimating Power Profiles of Mobile Workloads. Journal of Low<br>Power Electronics, 2012, 8, 293-303.   | 0.6 | 1         |
| 74 | Heuristic search strategies for multiobjective state space search. Sadhana - Academy Proceedings in<br>Engineering Sciences, 1996, 21, 263-290.                                       | 0.8 | 0         |
| 75 | Min-max event-triggered computation tree logic. Sadhana - Academy Proceedings in Engineering Sciences, 2002, 27, 163-180.   | 0.8 | Ο         |
| 76 | Property Driven Test Generation in Absence of Direct Interface. , 2006, , .   |     | 0         |
| 77 | A New Pseudo-Boolean Satisfiability based approach to Power Mode Schedulability Analysis. , 2007, , .   |     | Ο         |
| 78 | Incremental Verification Techniques for an Updated Architectural Specification. , 2009, , .   |     | 0         |
| 79 | Directed automated symbolic verification of formal properties with local variables. , 2009, , .   |     | 0         |
| 80 | Auto-generation of ams behavioral models in different languages from hybrid automata. , 2010, , .   |     | 0         |
| 81 | A study of modeling techniques in use in digital and mixed-signal domains for semi-formal verification. , 2010, , .   |     | ο         |
| 82 | Backward Reasoning with Formal Properties: A Methodology for Bug Isolation on Simulation Traces. ,<br>2011, , .   |     | 0         |
| 83 | POWER-SIM: An SOC Simulator for Estimating Power Profiles of Mobile Workloads. , 2011, , .  |     | 0         |
| 84 | A Library for Passive Online Verification of Analog and Mixed-Signal Circuits. , 2012, , .  |     | 0         |
| 85 | Acceptance and random generation of event sequences under real time calculus constraints. , 2014, , .   |     | 0         |
| 86 | Formal Methods for Coverage Analysis of Power Management Logic with Mixed-Signal Components. ,<br>2018, , .   |     | 0         |
| 87 | Usage-Driven Personalization of Power Management Logic. IEEE Embedded Systems Letters, 2021, 13, 106-109.   | 1.3 | 0         |
| 88 | Performance-Driven Post-Processing of Control Loop Execution Schedules. ACM Transactions on Design Automation of Electronic Systems, 2021, 26, 1-27.                                  | 1.9 | 0         |
| 89 | Exploitable Fault Space Characterization: A Complementary Approach. , 2019, , 59-88.  |     | 0         |
| 90 | CoVerPlan: A <u>Co</u> mprehensive <u>Ver</u> ification <u>Plan</u> ning Framework leveraging PSS Specifications. ACM Transactions on Design Automation of Electronic Systems, 0, , . | 1.9 | 0         |