

Zhufei Chu

List of Publications by Year in descending order

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Version: 2024-02-01

32
papers

138
citations

1478505

6
h-index

1372567

10
g-index

32
all docs

32
docs citations

32
times ranked

69
citing authors

#	ARTICLE	IF	CITATIONS
1	Through-Silicon Via-Based Capacitor and Its Application in LDO Regulator Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1947-1951.	3.1	23
2	An Integrated Optimization Approach for Nanohybrid Circuit Cell Mapping. IEEE Nanotechnology Magazine, 2011, 10, 1275-1284.	2.0	16
3	Advanced Functional Decomposition Using Majority and Its Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1621-1634.	2.7	12
4	BCD Adder Designs Based on Three-Input XOR and Majority Gates. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1942-1946.	3.0	10
5	CMOL cell assignment by genetic algorithm. , 2010, , .		9
6	A Memetic Approach for Nanoscale Hybrid Circuit Cell Mapping. , 2010, , .		8
7	Efficient nonrectangular shaped voltage island aware floorplanning with nonrandomized searching engine. Microelectronics Journal, 2014, 45, 382-393.	2.0	7
8	Functional decomposition using majority. , 2018, , .		7
9	Exact Synthesis of Boolean Functions in Majority-of-Five Forms. , 2019, , .		7
10	A High-Performance Design of Generalized Pipeline Cellular Array. IEEE Computer Architecture Letters, 2020, 19, 47-50.	1.5	6
11	Logic Synthesis Optimization Sequence Tuning Using RL-Based LSTM and Graph Isomorphism Network. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3600-3604.	3.0	5
12	Timing-driven logic restructuring for nano-hybrid circuits. International Journal of Electronics, 2013, 100, 669-685.	1.4	3
13	Multi-supply voltage (MSV) driven SoC floorplanning for fast design convergence. The Integration VLSI Journal, 2016, 52, 335-346.	2.1	3
14	Improving Circuit Mapping Performance Through MIG-based Synthesis for Carry Chains. , 2017, , .		3
15	Multi-objective algebraic rewriting in XOR-majority graphs. The Integration VLSI Journal, 2019, 69, 40-49.	2.1	3
16	MinSC: An Exact Synthesis-Based Method for Minimal-Area Stochastic Circuits under Relaxed Error Bound. , 2021, , .		3
17	Efficient Design of Decimal Full Adder Using Quantum-dot Cellular Automata. , 2018, , .		2
18	T-Channel Field Effect Transistor with Three Input Terminals (Ti-TcFET). Micromachines, 2020, 11, 64.	2.9	2

#	ARTICLE	IF	CITATIONS
19	Generic algorithm based voltage Islands-Aware Multiple Voltage Assignment. , 2010, , .		1
20	Voltage Drop Aware Power Pad Assignment and Floorplanning for Multi-voltage SoC Designs. , 2013, , .		1
21	Level shifter planning for timing constrained multi-voltage SoC floorplanning. , 2014, , .		1
22	Efficient power pad assignment for multi-voltage SoC and its application in floorplanning. International Journal of Circuit Theory and Applications, 2016, 44, 1533-1550.	2.0	1
23	A Novel Toffoli Gate Design Using Quantum-dot Cellular Automata. , 2021, , .		1
24	Design of Majority Logic Based 4-bit Approximate Subtractors and its Application in Divider. , 2021, , .		1
25	Area Optimization of Circuits Using Approximate Computing. , 2020, , .		1
26	Design and evaluation of approximate adders. , 2020, , .		1
27	Wire-Crossings Optimization Based on Majority-of-Five and XOR-of-Three Primitives in QCA. International Journal of Theoretical Physics, 2022, 61, 1.	1.2	1
28	CMOL cell assignment based on dynamic interchange. , 2009, , .		0
29	The efficient prediction technique of SAR based on a modified FDTD method. , 2015, , .		0
30	Area Optimization of MPRM Circuits Using Approximate Computing. , 2019, , .		0
31	An Efficient Demultiplexer Design in Quantum-dot Cellular Automata. , 2021, , .		0
32	Stochastic circuit synthesis via satisfiability. The Integration VLSI Journal, 2022, 84, 84-91.	2.1	0