MarÃ-a Teresa Serrano Gotarredona

List of Publications by Year
in descending order

92 papers	4,948 citations	212478 28 h-index	129628 63 g-index
94 all docs	94 docs citations	94 times ranked	4188 citing authors

#	Article	IF	Citations
1	A CMOSâ€“memristor hybrid system for implementing stochastic binary spike timing-dependent plasticity. Philosophical Transactions Series A, Mathematical, Physical, and Engineering Sciences, 2022, 380, .	1.6	6
2	Neuromorphic Sensors, Vision. , 2022, , 2340-2344.		0
3	Neuromorphic Low-Power Inference on Memristive Crossbars With On-Chip Offset Calibration. IEEE Access, 2021, 9, 38043-38061.	2.6	11
4	Foveal-pit inspired filtering of DVS spike response. , 2021, , .		1
5	On- and Off-centre Pathways in a Retina-Cerebellum Spiking Neural Network on SpiNNaker**This work is supported by the Science and Engineering Research Board of India (SERB) Core Research Grant CRG/2019/003534, BITS Pilani Institutional Research Grants GOA/ACG/2019-20/Oct/02 and BPGC/RIG/2018-19. TSG is supported by EU grant PCI2019-111826-2 â€œAPROVIS3Dâ€, by Spanish grant from the Ministry of Science and Innovation PID2019-105556GB-C31 â€œNANOMINDâ€• (with support from the) Ti ETOg1 1 0.784314 rgBT /Ove		1
6	A Reduced-Scale Cortical Network with Izhikevich's Neurons on SpiNNaker. , 2021, , .		1
7	Hardware Implementation of Differential Oscillatory Neural Networks Using VO 2-Based Oscillators and Memristor-Bridge Circuits. Frontiers in Neuroscience, 2021, 15, 674567.	1.4	20
8	Experimental Body-Input Three-Stage DC Offset Calibration Scheme for Memristive Crossbar. , 2020, , .		1
9	Introduction to the Special Issue on the 2nd IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS 2020). IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 403-405.	2.7	1
10	Implementation of a tunable spiking neuron for STDP with memristors in FDSOI 28nm. , 2020, , .		2
11	Enhanced Linearity in FD-SOI CMOS Body-Input Analog Circuits â€“ Application to Voltage-Controlled Ring Oscillators and Frequency-Based Î£Î” ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3297-3308.	3.5	6
12	Introduction and Analysis of an Event-Based Sign Language Dataset. , 2020, , .		12
13	Auxiliary Pulse-Extender and Current-Attenuator Circuits for Flexible Interaction with Memristive Crossbars in SNNs. , 2020, , .		1
14	A Current-Attenuator for Performing Read Operation in Memristor-Based Spiking Neural Networks. , 2020, , .		0
15	A Digital Neuromorphic Realization of the 2-D Wilson Neuron Model. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 136-140.	2.2	18
16	Asynchronous Spiking Neurons, the Natural Key to Exploit Temporal Sparsity. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 668-678.	2.7	15
17	Conversion of Synchronous Artificial Neural Network to Asynchronous Spiking Neural Network using sigma-delta quantization. , 2019, , .		17
18	Neuromorphic Spiking Neural Networks and Their Memristor-CMOS Hardware Implementations. Materials, 2019, 12, 2745.	1.3	71

#	Article	IF	Citations
19	Low-power hardware implementation of SNN with decision block for recognition tasks. , 2019, , .		5
20	Spike-Timing-Dependent-Plasticity withÂMemristors. , 2019, , 429-467.		2
21	Spiking Hough for Shape Recognition. Lecture Notes in Computer Science, 2018, , 425-432.	1.0	1
22	Hybrid Neural Network, An Efficient Low-Power Digital Hardware Implementation of Event-based Artificial Neural Network. , 2018, , .		11
23	Event-Driven Stereo Visual Tracking Algorithm to Solve Object Occlusion. IEEE Transactions on Neural Networks and Learning Systems, 2018, 29, 4223-4237.	7.2	34
24	Scene Context Classification with Event-Driven Spiking Deep Neural Networks. , 2018, , .		2
25	On Practical Issues for Stochastic STDP Hardware With 1-bit Synaptic Weights. Frontiers in Neuroscience, 2018, 12, 665.	1.4	49
26	A Configurable Event-Driven Convolutional Node with Rate Saturation Mechanism for Modular ConvNet Systems Implementation. Frontiers in Neuroscience, 2018, 12, 63.	1.4	23
27	Performance Comparison of Time-Step-Driven versus Event-Driven Neural State Update Approaches in SpiNNaker. , 2018, , .		2
28	Active Perception With Dynamic Vision Sensors. Minimum Saccades With Optimum Recognition. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 927-939.	2.7	16
29	On Multiple AER Handshaking Channels Over High-Speed Bit-Serial Bidirectional LVDS Links With Flow-Control and Clock-Correction on Commercial FPGAs for Scalable Neuromorphic Systems. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1133-1147.	2.7	30
30	An Event-Driven Classifier for Spiking Neural Networks Fed with Synthetic or Dynamic Vision Sensor Data. Frontiers in Neuroscience, 2017, 11, 350.	1.4	78
31	A Spiking Neural Network Model of the Lateral Geniculate Nucleus on the SpiNNaker Machine. Frontiers in Neuroscience, 2017, 11, 454.	1.4	9
32	Benchmarking Spike-Based Visual Recognition: A Dataset and Evaluation. Frontiers in Neuroscience, 2016, 10, 496.	1.4	27
33	Fast Predictive Handshaking in Synchronous FPGAs for Fully Asynchronous Multisymbol Chip Links: Application to SpiNNaker 2-of-7 Links. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 763-767.	2.2	9
34	Plasticity in memristive devices for spiking neural networks. Frontiers in Neuroscience, 2015, 9, 51.	1.4	188
35	Poker-DVS and MNIST-DVS. Their History, How They Were Made, and Other Details. Frontiers in Neuroscience, 2015, 9, 481.	1.4	88
36	On the use of orientation filters for 3D reconstruction in event-driven stereo vision. Frontiers in Neuroscience, 2014, 8, 48.	1.4	25

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37	Spike-Timing-Dependent-Plasticity in Hybrid Memristive-CMOS Spiking Neuromorphic Systems. , 2014, , 353-377.		1
38	Spike-based VITE control with dynamic vision sensor applied to an arm robot. , 2014, , .		5
39	Retinomorphic Event-Based Vision Sensors: Bioinspired Cameras With Spiking Output. Proceedings of the IEEE, 2014, 102, 1470-1484.	16.4	270
40	A Proposal for Hybrid Memristor-CMOS Spiking Neuromorphic Learning Systems. IEEE Circuits and Systems Magazine, 2013, 13, 74-88.	2.6	56
41	A 128$,imes$128 1.5% Contrast Sensitivity 0.9% FPN 3 Âµs Latency 4 mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Preamplifiers. IEEE Journal of Solid-State Circuits, 2013, 48, 827-838.	3.5	268
42	Mapping from Frame-Driven to Frame-Free Event-Driven Vision Systems by Low-Rate Rate Coding and Coincidence Processing–Application to Feedforward ConvNets. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2013, 35, 2706-2719.	9.7	230
43	Multicasting Mesh AER: A Scalable Assembly Approach for Reconfigurable Neuromorphic Structured AER Systems. Application to ConvNets. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 82-102.	2.7	83
44	A 1.5 ns OFF/ON Switching-Time Voltage-Mode LVDS Driver/Receiver Pair for Asynchronous AER Bit-Serial Chip Grid Links With Up to 40 Times Event-Rate Dependent Power Savings. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 722-731.	2.7	3
45	An Event-Driven Multi-Kernel Convolution Processor Module for Event-Driven Vision Sensors. IEEE Journal of Solid-State Circuits, 2012, 47, 504-517.	3.5	92
46	A Real-Time, Event-Driven Neuromorphic System for Goal-Directed Attentional Selection. Lecture Notes in Computer Science, 2012, , 226-233.	1.0	17
47	A <formula formulatype="inline"><tex Notation="TeX">${0.35}~mu{m m}$</tex></formula> Sub-ns Wake-up Time ON-OFF Switchable LVDS Driver-Receiver Chip I/O Pad Pair for Rate-Dependent Power Saving in AER Bit-Serial Links. IEEE Transactions on Biomedical Circuits and Systems, 2012, 6, 486-497.	2.7	14
48	Comparison between Frame-Constrained Fix-Pixel-Value and Frame-Free Spiking-Dynamic-Pixel ConvNets for Visual Processing. Frontiers in Neuroscience, 2012, 6, 32.	1.4	54
49	A Memristive Nanoparticle/Organic Hybrid Synapstor for Neuroinspired Computing. Advanced Functional Materials, 2012, 22, 609-616.	7.8	163
50	A 32$,imes,$32 Pixel Convolution Processor Chip for Address Event Vision Sensors With 155 ns Event Latency and 20 Meps Throughput. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 777-790.	3.5	47
51	Neuromorphic Silicon Neuron Circuits. Frontiers in Neuroscience, 2011, 5, 73.	1.4	1,004
52	A 3.6 mus Latency Asynchronous Frame-Free Event-Driven Dynamic-Vision-Sensor. IEEE Journal of Solid-State Circuits, 2011, 46, 1443-1455.	3.5	196
53	An Instant-Startup Jitter-Tolerant Manchester-Encoding Serializer/Deserializer Scheme for Event-Driven Bit-Serial LVDS Interchip AER Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2647-2660.	3.5	17
54	On Spike-Timing-Dependent-Plasticity, Memristive Devices, and Building a Self-Learning Visual Cortex. Frontiers in Neuroscience, 2011, 5, 26.	1.4	364

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55	Voltage mode driver for low power transmission of high speed serial AER Links. , 2011, , .		4
56	Spike-Based Convolutional Network for Real-Time Processing. , 2010, , .		13
57	Fast Vision Through Frameless Event-Based Sensing and Convolutional Processing: Application to Texture Recognition. IEEE Transactions on Neural Networks, 2010, 21, 609-620.	4.8	32
58	A Five-Decade Dynamic-Range Ambient-Light-Independent Calibrated Signed-Spatial-Contrast AER Retina With 0.1-ms Latency and Optional Time-to-First-Spike Mode. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2632-2643.	3.5	34
59	OTA-C oscillator with low frequency variations for on-chip clock generation in serial LVDS-AER links. , 2009, , .		2
60	CAVIAR: A 45k Neuron, 5M Synapse, 12G Connects/s AER Hardware Sensoryâ€“Processingâ€“ Learningâ€“Actuating System for High-Speed Visual Object Recognition and Tracking. IEEE Transactions on Neural Networks, 2009, 20, 1417-1438.	4.8	285
61	A weak-to-strong inversion mismatch model for analog circuit design. Analog Integrated Circuits and Signal Processing, 2009, 59, 325-340.	0.9	3
62	Advanced Vision Processing Systems: Spike-Based Simulation and Processing. Lecture Notes in Computer Science, 2009, , 640-651.	1.0	4
63	A Calibration Technique for Very Low Current and Compact Tunable Neuromorphic Cells: Application to 5-bit 20-nA DACs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 522-526.	2.2	16
64	On Real-Time AER 2-D Convolutions Hardware for Neuromorphic Spike-Based Cortical Processing. IEEE Transactions on Neural Networks, 2008, 19, 1196-1219.	4.8	65
65	Compact calibration circuit for large neuromorphic arrays. , 2008, , .		0
66	Fully digital AER convolution chip for vision processing. , 2008, , .		9
67	LVDS interface for AER links with burst mode operation capability. , 2008, , .		6
68	An Accurate Automatic Quality-Factor Tuning Scheme for Second-Order <emphasis emphasistype="italic">LC</emphasis> Filters. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 745-756.	0.1	7
69	The Stochastic I-Pot: A Circuit Block for Programming Bias Currents. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 760-764.	2.2	20
70	A Spatial Contrast Retina With On-Chip Calibration for Neuromorphic Spike-Based AER Vision Systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1444-1458.	0.1	90
71	A Neuromorphic Cortical-Layer Microchip for Spike-Based Event Processing Vision Systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 2548-2566.	0.1	88
72	A Low-Power Current Mode Fuzzy-ART Cell. IEEE Transactions on Neural Networks, 2006, 17, 1666-1673.	4.8	6

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73	A calibration scheme for subthreshold current mode circuits. , 2005, , .		0
74	A digital pixel cell for address event representation image convolution processing. , 2005, , .		2
75	Event generators for address event representation transmitters. , 2005, 5839, 148.		4
76	Current Mode Techniques for Sub-pico-Ampere Circuit Design. Analog Integrated Circuits and Signal Processing, 2004, 38, 103-119.	0.9	30
77	Precise 90Â° quadrature current-controlled oscillator tunable between 50â€“130â€…MHz. Electronics Letters, 2003, 39, 823.	0.5	0
78	On the design and characterization of femtoampere current-mode circuits. IEEE Journal of Solid-State Circuits, 2003, 38, 1353-1363.	3.5	161
79	Log-domain implementation of complex dynamics reaction-diffusion neural networks. IEEE Transactions on Neural Networks, 2003, 14, 1337-1355.	4.8	40
80	Compact low-power calibration mini-DACs for neural arrays with programmable weights. IEEE Transactions on Neural Networks, 2003, 14, 1207-1216.	4.8	44
81	Current-mode fully-programmable piece-wise-linear block for neuro-fuzzy applications. Electronics Letters, 2002, 38, 1165.	0.5	14
82	A Programmable VLSI Filter Architecture for Application in Real-Time Vision Processing Systems. International Journal of Neural Systems, 2000, 10, 179-190.	3.2	4
83	A new five-parameter MOS transistor mismatch model. IEEE Electron Device Letters, 2000, 21, 37-39.	2.2	24
84	Systematic Width-and-Length Dependent CMOS Transistor Mismatch Characterization and Simulation. Analog Integrated Circuits and Signal Processing, 1999, 21, 271-296.	0.9	42
85	Bipolar/CMOS current-source flip-flop for application in neuro-fuzzy systems. Electronics Letters, 1999, 35, 1326.	0.5	2
86	Adaptive resonance theory microchips. Lecture Notes in Computer Science, 1999, , 737-746.	1.0	8
87	7-decade tuning range CMOS OTA-C sinusoidal VCO. Electronics Letters, 1998, 34, 1621.	0.5	16
88	An ART1 microchip and its use in multi-ART1 systems. IEEE Transactions on Neural Networks, 1997, 8, 1184-1194.	4.8	17
89	A real-time clustering microchip neural engine. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1996, 4, 195-209.	2.1	23
90	A Modified ART 1 Algorithm more Suitable for VLSI Implementations. Neural Networks, 1996, 9, 1025-1043.	3.3	26

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91	Memristance can explain Spike-Time-Dependent-Plasticity in Neural Synapses. Nature Precedings, 0, , .	0.1	128
92	SL-Animals-DVS: event-driven sign language animals dataset. Pattern Analysis and Applications, 0, , 1.	3.1	5