Jeevan Battini

List of Publications by Year
in descending order

6	32	3	3
papers	citations	h-index	g-index

6	6	6	15
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 16 nm FinFET circuit with triple function as digital multiplexer, active-high and active-low output decoder for high-performance SRAM architecture. Semiconductor Science and Technology, 2022, 37, 085021.	2.0	5
2	Design of 0.8V, 22 nm DG-FinFET based efficient VLSI multiplexers. Microelectronics Journal, 2021, 113, 105059.	2.0	4
3	A New High-Speed Multiplier Based on Carry-Look-Ahead Adder and Compressor. Lecture Notes in Electrical Engineering, 2018, , 69-78.	0.4	5
4	A Review on different Logic Styles to design High Performance VLSI Decoders. , 2018, , .		3
5	FPGA implementation of secure image compression with 2D-DCT using Verilog HDL. , 2014, , .		4
6	A high speed binary floating point multiplier using Dadda algorithm. , 2013, , .		11