

Jeevan Battini

List of Publications by Year in descending order

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Version: 2024-02-01

6
papers

32
citations

2258059

3
h-index

2550090

3
g-index

6
all docs

6
docs citations

6
times ranked

15
citing authors

#	ARTICLE	IF	CITATIONS
1	A high speed binary floating point multiplier using Dadda algorithm. , 2013, , .		11
2	A New High-Speed Multiplier Based on Carry-Look-Ahead Adder and Compressor. Lecture Notes in Electrical Engineering, 2018, , 69-78.	0.4	5
3	A 16â€nm FinFET circuit with triple function as digital multiplexer, active-high and active-low output decoder for high-performance SRAM architecture. Semiconductor Science and Technology, 2022, 37, 085021.	2.0	5
4	FPGA implementation of secure image compression with 2D-DCT using Verilog HDL. , 2014, , .		4
5	Design of 0.8V, 22Ânm DG-FinFET based efficient VLSI multiplexers. Microelectronics Journal, 2021, 113, 105059.	2.0	4
6	A Review on different Logic Styles to design High Performance VLSI Decoders. , 2018, , .		3