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List of Publications by Year
in descending order

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38 papers	785 citations	759233 12 h-index	526287 27 g-index
38 all docs	38 docs citations	38 times ranked	612 citing authors

#	Article	IF	Citations
1	Compact model for short channel symmetric doped double-gate MOSFETs. Solid-State Electronics, 2008, 52, 1064-1070.	1.4	140
2	New procedure for the extraction of basic a-Si:H TFT model parameters in the linear and saturation regions. Solid-State Electronics, 2001, 45, 1077-1080.	1.4	134
3	Mobility model for compact device modeling of OTFTs made with different materials. Solid-State Electronics, 2008, 52, 787-794.	1.4	89
4	Charge based DC compact modeling of bulk FinFET transistor. Solid-State Electronics, 2013, 87, 11-16.	1.4	63
5	Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs. Solid-State Electronics, 2008, 52, 830-837.	1.4	62
6	Integral function method for determination of nonlinear harmonic distortion. Solid-State Electronics, 2004, 48, 2225-2234.	1.4	59
7	New procedure for the extraction of a-Si:H TFTs model parameters in the subthreshold region. Solid-State Electronics, 2003, 47, 1351-1358.	1.4	33
8	A compact model and direct parameters extraction techniques For amorphous gallium-indium-zinc-oxide thin film transistors. Solid-State Electronics, 2016, 126, 81-86.	1.4	24
9	Organic thin-film transistor bias-dependent capacitance compact model in accumulation regime. IET Circuits, Devices and Systems, 2012, 6, 130.	1.4	23
10	Modeling the behavior of amorphous oxide thin film transistors before and after bias stress. Microelectronics Reliability, 2012, 52, 2532-2536.	1.7	20
11	DC self-heating effects modelling in SOI and bulk FinFETs. Microelectronics Journal, 2015, 46, 320-326.	2.0	20
12	Compact Capacitance Model for OTFTs at Low and Medium Frequencies. IEEE Transactions on Electron Devices, 2014, 61, 638-642.	3.0	13
13	High-frequency compact analytical noise model for double-gate metal-oxide-semiconductor field-effect transistor. Journal of Applied Physics, 2009, 105, 034510.	2.5	10
14	An insight to mobility parameters for AOSTFTs, when the effect of both, localized and free carriers, must be considered to describe the device behavior. Solid-State Electronics, 2018, 149, 32-37.	1.4	10
15	A Complete Charge-Based Capacitance Model for IGZO TFTs. IEEE Electron Device Letters, 2019, 40, 730-733.	3.9	10
16	Non-linear performance comparison for FD and PD SOI MOSFETs based on the integral function method and Volterra modelling. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2005, 18, 283-296.	1.9	8
17	3D simulation of triple-gate MOSFETs with different mobility regions. Microelectronic Engineering, 2011, 88, 1633-1636.	2.4	8
18	New Compact Modeling Solutions for Organic and Amorphous Oxide TFTs. IEEE Journal of the Electron Devices Society, 2021, 9, 911-932.	2.1	8

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19	Pseudo-Boltzmann model for modeling the junctionless transistors. Solid-State Electronics, 2014, 95, 19-22.	1.4	7
20	Full capacitance model, considering the specifics of amorphous oxide semiconductor thin film transistors structures. Solid-State Electronics, 2019, 156, 16-22.	1.4	7
21	Analytical Currentâ€“Voltage Model for Double-Gate a-IGZO TFTs With Symmetric Structure for Above Threshold. IEEE Transactions on Electron Devices, 2020, 67, 1980-1986.	3.0	5
22	Review on double-gate MOSFETs and FinFETs modeling. Facta Universitatis - Series Electronics and Energetics, 2013, 26, 197-213.	0.9	5
23	Parameter Extraction and Compact Modeling of OTFTs From 150 K to 350 K. IEEE Transactions on Electron Devices, 2020, 67, 5685-5692.	3.0	5
24	Nonlinearity Analysis of FinFETs. , 2006, , .		4
25	Gate leakage currents modeling for oxynitride gate dielectric in double gate MOSFETs. , 2011, , .		4
26	Compact DC and Quasi-Static Capacitances Modeling of a-Si:H TFTs, Including Parasitic Capacitances. IEEE Transactions on Electron Devices, 2021, 68, 3384-3389.	3.0	4
27	Mathematical basis of the expressions used by the integral function method for the determination of nonlinear hannonic distortion in devices and circuits. , 0, , .		2
28	Graded-Channel SOI nMOSFET Model Valid for Harmonic Distortion Evaluation. , 0, , .		2
29	On the compact modelling of Si nanowire and Si nanosheet MOSFETs. Semiconductor Science and Technology, 2022, 37, 025014.	2.0	2
30	Linearity study of DG MOSFETs. , 2009, , .		1
31	Temperature dependence of compact analytical modeling of gate tunneling current in Double Gate MOSFETs. , 2012, , .		1
32	Features of the Nonlinear Harmonic Distortion in AOSTFTs. IEEE Transactions on Electron Devices, 2019, 66, 5177-5182.	3.0	1
33	Dynamic Simulation of a-IGZO TFT Circuits Using the Analytical Full Capacitance Model (AFCM). IEEE Journal of the Electron Devices Society, 2021, 9, 464-468.	2.1	1
34	A Modified EKV PDSOI MOSFETs Model. , 0, , .		0
35	A High Frequency Compact Noise Model for Double-Gate MOSFET Devices. , 2009, , .		0
36	DC thermal numerical simulation of DG MOSFET. , 2011, , .		0

#	Article	IF	Citations
37	Bias stress study of Metal-Insulator-Semiconductor structures with pulsed laser deposited InGaZnO on atomic layer deposited HfO2. , 2015, , .		0
38	Analytical I-V and C-V models for symmetric double-gate AOSTFTs. Semiconductor Science and Technology, 0, , .	2.0	0