Michael P Flynn

List of Publications by Year
in descending order

54 papers	1,842 citations	394286 19 h-index	345118 36 g-index
55 all docs	55 docs citations	55 times ranked	1913 citing authors

#	Article	IF	Citations
1	An Eight-Element Frequency-Selective Acoustic Beamformer and Bitstream Feature Extractor. IEEE Journal of Solid-State Circuits, 2022, 57, 1812-1823.	3.5	3
2	TAICHI: A Tiled Architecture for In-Memory Computing and Heterogeneous Integration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 559-563.	2.2	5
3	A Multimode 157Î¼W 4-Channel 80dBA-SNDR Speech-Recognition Frontend With Self-DOA Correction Adaptive Beamformer. , 2022, , .		2
4	A 17.8-MS/s Compressed Sensing Radar Accelerator Using a Spiking Neural Network. IEEE Journal of Solid-State Circuits, 2021, 56, 834-843.	3.5	2
5	A Hybrid-Loop Structure and Interleaved Noise-Shaped Quantizer for a Robust 100-MHz BW and 69-dB DR DSM. IEEE Journal of Solid-State Circuits, 2021, 56, 3681-3693.	3.5	2
6	A 16-Element Fully Integrated 28-GHz Digital RX Beamforming Receiver. IEEE Journal of Solid-State Circuits, 2021, 56, 1374-1386.	3.5	21
7	A 6-GHz MU-MIMO Eight-Element Direct Digital Beamforming TX Utilizing FIR H-Bridge DAC. IEEE Transactions on Microwave Theory and Techniques, 2021, 69, 2832-2840.	2.9	7
8	Erratum to â€œA 16-Element Fully Integrated 28-GHz Digital RX Beamforming Receiverâ€• IEEE Journal of Solid-State Circuits, 2021, 56, 3204-3204.	3.5	0
9	TaNS-DDRF: A 160-MHz Bandwidth 6-GHz Carrier Frequency Digital-Direct RF Transmitter for Wi-Fi 6E with Targeted Noise-Shaping. , 2021, , .		1
10	An Overview of Noise-Shaping SAR ADC: From Fundamentals to the Frontier. IEEE Open Journal of the Solid-State Circuits Society, 2021, 1, 149-161.	2.0	15
11	A secure measurement unit for an inspection system used in nuclear arms-control verification. Nuclear Instruments and Methods in Physics Research, Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 2020, 982, 164577.	0.7	0
12	A Cascaded Noise-Shaping SAR Architecture for Robust Order Extension. IEEE Journal of Solid-State Circuits, 2020, 55, 3236-3247.	3.5	29
13	A Fully Integrated Reprogrammable CMOS-RRAM Compute-in-Memory Coprocessor for Neuromorphic Applications. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 36-44.	1.1	20
14	A fully integrated reprogrammable memristorâ€“CMOS system for efficient multiplyâ€“accumulate operations. Nature Electronics, 2019, 2, 290-299.	13.1	469
15	A Two-Beam Eight-Element Direct Digital Beamforming RF Modulator in 40-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2019, 67, 2569-2579.	2.9	8
16	A Simultaneous Multiband Continuous-Time $DeltaSigma$ ADC With 90-MHz Aggregate Bandwidth in 40-nm CMOS. IEEE Solid-State Circuits Letters, 2019, 2, 91-94.	1.3	4
17	A 77dB-SFDR Multi-Phase-Sampling 16-Element Digital Beamformer with 64 4GS/s 100MHz-BW Continuous-Time Band-Pass Î”Î£ ADCs. , 2019, , .		3
18	A Calibration-Free Time-Interleaved Fourth-Order Noise-Shaping SAR ADC. IEEE Journal of Solid-State Circuits, 2019, 54, 3386-3395.	3.5	25

#	Article	IF	Citations
19	Design Considerations for Integrated Radar Chirp Synthesizers. IEEE Access, 2019, 7, 13723-13736.	2.6	5
20	20.3 A 50MHz-Bandwidth 70.4dB-SNDR Calibration-Free Time-Interleaved 4th-Order Noise-Shaping SAR ADC. , 2019, , .		15
21	A 1-GHz 16-Element Four-Beam True-Time-Delay Digital Beamformer. IEEE Journal of Solid-State Circuits, 2019, 54, 1304-1314.	3.5	41
22	A Simultaneous Multiband Continuous-Time Î”Î£ ADC With 90-MHz Aggregate Bandwidth in 40-nm CMOS. , 2019, , .		1
23	Digital Fractional-<inline-formula> <tex-math notation="LaTeX">N </tex-math> </inline-formula> PLLs Based on a Continuous-Time Third-Order Noise-Shaping Time-to-Digital Converter for a 240-GHz FMCW Radar System. IEEE Journal of Solid-State Circuits, 2018, 53, 1719-1730.	3.5	13
24	A 16-Element 4-Beam 1 GHz IF 100 MHz Bandwidth Interleaved Bit Stream Digital Beamformer in 40 nm CMOS. IEEE Journal of Solid-State Circuits, 2018, 53, 1302-1312.	3.5	15
25	A Mismatch-Immune 12-Bit SAR ADC With Completely Reconfigurable Capacitor DAC. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1589-1593.	2.2	2
26	A Maximum-Likelihood Sequence Detection Powered ADC-Based Serial Link. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2269-2278.	3.5	9
27	A calibration-free 2.3 mW 73.2 dB SNDR 15b 100 MS/s four-stage fully differential ring amplifier based SAR-assisted pipeline ADC. , 2017, , .		32
28	A 69 dB SNDR, 25 MHz BW, 800 MS/s Continuous-Time Bandpass Modulator Using a Duty-Cycle-Controlled DAC for Low Power and Reconfigurability. IEEE Journal of Solid-State Circuits, 2016, 51, 649-659.	3.5	19
29	A 260 MHz IF Sampling Bit-Stream Processing Digital Beamformer With an Integrated Array of Continuous-Time Band-Pass Modulators. IEEE Journal of Solid-State Circuits, 2016, 51, 1168-1176.	3.5	31
30	New Associate Editor. IEEE Journal of Solid-State Circuits, 2016, 51, 571-571.	3.5	0
31	Introducing BrowZine, a Tablet and Phone-Based Reader for the JSSC. IEEE Journal of Solid-State Circuits, 2016, 51, 572-572.	3.5	0
32	Introducing Short Regular Papers. IEEE Journal of Solid-State Circuits, 2016, 51, 573-573.	3.5	0
33	An IF 8-element 2-beam bit-stream band-pass beamformer. , 2015, , .		1
34	26.1 A 1mW 71.5dB SNDR 50MS/S 13b fully differential ring-amplifier-based SAR-assisted pipeline ADC. , 2015, , .		19
35	A 28.5–33.5GHz fractional-N PLL using a 3rd order noise shaping time-to-digital converter with 176fs resolution. , 2015, , .		4
36	A 1 mW 71.5 dB SNDR 50 MS/s 13 bit Fully Differential Ring Amplifier Based SAR-Assisted Pipeline ADC. IEEE Journal of Solid-State Circuits, 2015, 50, 2901-2911.	3.5	126

#	Article	IF	Citations
37	New Associate Editors. IEEE Journal of Solid-State Circuits, 2014, 49, 1459-1459.	3.5	0
38	A 12 mW Low Power Continuous-Time Bandpass Î”Î£ Modulator With 58 dB SNDR and 24 MHz Bandwidth at 200 MHz IF. IEEE Journal of Solid-State Circuits, 2014, 49, 405-415.	3.5	47
39	A Fully Self-Contained Logarithmic Closed-Loop Deep Brain Stimulation SoC With Wireless Telemetry and Wireless Power Management. IEEE Journal of Solid-State Circuits, 2014, 49, 2213-2227.	3.5	87
40	A Low-Power Adaptive Receiver Utilizing Discrete-Time Spectrum-Sensing. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 1338-1346.	2.9	6
41	A 90-MS/s 11-MHz-Bandwidth 62-dB SNDR Noise-Shaping SAR ADC. IEEE Journal of Solid-State Circuits, 2012, 47, 2898-2904.	3.5	182
42	Statistical Analysis of ENOB and Yield in Binary Weighted ADCs and DACS With Random Element Mismatch. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 1396-1408.	3.5	36
43	A Low-Power Compressive Sampling Time-Based Analog-to-Digital Converter. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 502-515.	2.7	18
44	A wirelessly powered log-based closed-loop deep brain stimulation SoC with two-way wireless telemetry for treatment of neurological disorders. , 2012, , .		8
45	A 2.4GHz 2Mb/s digital PLL-based transmitter for 802.15.4 in 130nm CMOS. , 2011, , .		2
46	A SAR-Assisted Two-Stage Pipeline ADC. IEEE Journal of Solid-State Circuits, 2011, 46, 859-869.	3.5	177
47	A 1.5-GS/s Flash ADC With 57.7-dB SFDR and 6.4-Bit ENOB in 90 nm Digital CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 837-841.	2.2	46
48	A 64 Channel Programmable Closed-Loop Neurostimulator With 8 Channel Neural Amplifier and Logarithmic ADC. IEEE Journal of Solid-State Circuits, 2010, 45, 1935-1945.	3.5	121
49	A 9-Gbit/s Serial Transceiver for On-Chip Global Signaling Over Lossy Transmission Lines. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1807-1817.	3.5	23
50	A 2.5 mW 80 dB DR 36 dB SNDR 22 MS/s Logarithmic Pipeline ADC. IEEE Journal of Solid-State Circuits, 2009, 44, 2755-2765.	3.5	37
51	A 4-GS/s 4-bit Flash ADC in 0.18-$mu{hbox {m}}$ CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 1865-1872.	3.5	91
52	ACHIEVING ANALOG ACCURACY IN NANOMETER CMOS. Selected Topics in Electornics and Systems, 2006, , 1-21.	0.2	1
53	Global High-Speed Signaling in Nanometer CMOS. , 2005, , .		4
54	ACHIEVING ANALOG ACCURACY IN NANOMETER CMOS. International Journal of High Speed Electronics and Systems, 2005, 15, 255-275.	0.3	6