Ramachandran Sakthivel

List of Publications by Year
in descending order

26	184	1307594 7	1281871 11
papers	citations	h-index	g-index

27	27	27	144
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Ultraâ€lowâ€voltage GDIâ€based hybrid full adder design for area and energyâ€efficient computing systems. IET Circuits, Devices and Systems, 2019, 13, 465-470.	1.4	33
2	High-performance ECC processor architecture design for IoT security applications. Journal of Supercomputing, 2019, 75, 447-474.	3.6	31
3	An efficient hardware implementation of the elliptic curve cryptographic processor over prime field,. International Journal of Circuit Theory and Applications, 2020, 48, 1256-1273.	2.0	21
4	Schmitt trigger-based single-ended 7T SRAM cell for Internet of Things (IoT) applications. Journal of Supercomputing, 2018, 74, 4613-4622.	3.6	18
5	15â€“4 Approximate Compressor Based Multiplier for Image Processing. , 2018, , .		9
6	Design of Artificial Neuron Network with Synapse Utilizing Hybrid CMOS Transistors with Memristor for Low Power Applications. Journal of Circuits, Systems and Computers, 2020, 29, 2050187.	1.5	9
7	An efficient hardware architecture based on an ensemble of deep learning models for COVID -19 prediction. Sustainable Cities and Society, 2022, 80, 103713.	10.4	9
8	Energy Efficient Low Area Error Tolerant Adder with Higher Accuracy. Circuits, Systems, and Signal Processing, 2014, 33, 2625-2641.	2.0	8
9	Low power high throughput reconfigurable stream cipher hardware VLSI architectures. International Journal of Information and Computer Security, 2014, 6, 1.	0.2	8
10	An optimized architecture to perform image compression and encryption simultaneously using modified DCT algorithm. , 2011, , .		6
11	Highly secured high throughput VLSI architecture for AES algorithm. , 2012, , .		6
12	Low power energy efficient pipelined multiply-accumulate architecture. , 2012, , .		5
13	Radix-4 Interleaved Modular Multiplication for Cryptographic Applications. , 2019, , .		4
14	Superior Implementation of Accelerated QR Decomposition for Ultrasound Imaging. IEEE Access, 2020, 8, 156244-156260.	4.2	3
15	A custom reconfigurable power efficient FIR filter. , 2016, , .		2
16	High Performance GCM Architecture for the Security of High Speed Network. International Journal of Parallel Programming, 2018, 46, 904-922.	1.5	2
17	Design of high quality factor fully-differential CMOS current conveyor for a complex filter application. , 2013, , .		1
18	A Low Power 10 bit 50-MS/s Sample and Hold OTA Amplifier. , 2018, , .		1

#	Article	IF	Citations
19	Neuron Network with a Synapse of CMOS transistor and Anti-Parallel Memristors for Low power Implementations. Journal of Circuits, Systems and Computers, 0, , .	1.5	1
20	An efficient VLSI architecture for variable threshold simple edge preserved denoising algorithm with improved signal to noise ratio. , 2011, , .		0
21	Design of dynamically reconfigurable fully optimized low power FFT architecture for MC-CDMA receiver. IEICE Electronics Express, 2013, 10, 20130252-20130252.	0.8	0
22	Implementation of Hierarchical DFT Approach for Better Testability. , 2018, , .		0
23	A Review On Dynamic Comparator Topologies. , 2019, , .		0
24	Single Bit Fault Detecting ALU Design using Reversible Gates. , 2020, , .		0
25	Low-Power Area Efficient Reconfigurable Pipelined Twoâ€™s Complement Multiplier with Reduced Error. Communications in Computer and Information Science, 2012, , 308-321.	0.5	0
26	Memristor Based CAM Cell Designs and Analaysis of Their Performance. , 2022, , .		0