

# Abhishek Nag

## List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	Design of Power Gated SRAM Cell for Reducing the NBTI Effect and Leakage Power Dissipation During the Hold Operation. Journal of Electronic Testing: Theory and Applications (JETTA), 2022, 38, 91-105.	1.2	4
2	Low power transistor level synthesis of finite state machines using a novel dual gating technique. International Journal of Embedded Systems, 2020, 13, 431.	0.3	0
3	Low-Power FSM Synthesis Based on Automated Power and Clock Gating Technique. Journal of Circuits, Systems and Computers, 2019, 28, 1920003.	1.5	4
4	Leakage Reduction of SRAM-Based Look-Up Table Using Dynamic Power Gating. Journal of Circuits, Systems and Computers, 2017, 26, 1750041.	1.5	7
5	Design of new high-speed and low-energy dynamic PLA. International Journal of Electronics Letters, 2016, 4, 87-92.	1.2	0
6	An Autonomous Clock Gating Technique in Finite State Machines Based on Registers Partitioning. Journal of Circuits, Systems and Computers, 2016, 25, 1650033.	1.5	5
7	CG-in-PG architecture implementation for power reduction in FSMs. International Journal of Electronics Letters, 2014, 2, 180-185.	1.2	2