Daniel Chaver

List of Publications by Year
in descending order

27 papers	152 citations	1684188 5 h-index	1281871 11 g-index
27 all docs	27 docs citations	27 times ranked	98 citing authors

#	Article	IF	Citations
1	RVfpga: Using a RISC-V Core Targeted to an FPGA in Computer Architecture Education. , 2021, , .		8
2	Reuse Detector: Improving the Management of STT-RAM SLLCs. Computer Journal, 2018, 61, 856-880.	2.4	3
3	Towards completely fair scheduling on asymmetric single-ISA multicore processors. Journal of Parallel and Distributed Computing, 2017, 102, 115-131.	4.1	20
4	MIPSfpga: using a commercial MIPS softâ€core in computer architecture education. IET Circuits, Devices and Systems, 2017, 11, 283-291.	1.4	15
5	Practical experiences based on MIPSfpga. , 2017, , .		1
6	An OS-Oriented Performance Monitoring Tool for Multicore Systems. Lecture Notes in Computer Science, 2015, , 697-709.	1.3	3
7	ACFS. , 2015, , .		10
8	Write-Aware Replacement Policies for PCM-Based Systems. Computer Journal, 2015, 58, 2000-2025.	2.4	5
9	IMPROVING peLIFO CACHE REPLACEMENT POLICY: HARDWARE REDUCTION AND THREAD-AWARE EXTENSION. Journal of Circuits, Systems and Computers, 2014, 23, 1450046.	1.5	0
10	Online Evaluation Methodology of Laboratory Sessions in Computer Science Degrees. Revista Iberoamericana De Tecnologias Del Aprendizaje, 2014, 9, 122-130.	0.9	7
11	Exploring the Throughput-Fairness Trade-off on Asymmetric Multicore Systems. Lecture Notes in Computer Science, 2014, , 326-337.	1.3	3
12	Delivering fairness and priority enforcement on asymmetric multicore systems via OS scheduling. , 2013, , .		3
13	Delivering fairness and priority enforcement on asymmetric multicore systems via OS scheduling. Performance Evaluation Review, 2013, 41, 343-344.	0.6	0
14	REDUCING CACHE HIERARCHY ENERGY CONSUMPTION BY PREDICTING FORWARDING AND DISABLING ASSOCIATIVE SETS. Journal of Circuits, Systems and Computers, 2012, 21, 1250057.	1.5	3
15	OpenIRS-UCM. , 2012, , .		3
16	Hybrid timing-address oriented load-store queue filtering for an x86 architecture. IET Computers and Digital Techniques, 2011, 5, 145.	1.2	1
17	Implementation of a hardware branch-predictor evaluation platform based on FPGAs. , 2009, , .		0
18	Using age registers for a simple loadâ€“store queue filtering. Journal of Systems Architecture, 2009, 55, 79-89.	4.3	2

#	Article	IF	Citations
19	Replacing Associative Load Queues: A Timing-Centric Approach. IEEE Transactions on Computers, 2009, 58, 496-511.	3.4	1
20	Energy reduction of the fetch mechanism through dynamic adaptation. IET Computers and Digital Techniques, 2008, 2, 94.	1.2	0
21	Substituting associative load queue with simple hash tables in out-of-order microprocessors. , 2006, , .		5
22	DMDC: Delayed Memory Dependence Checking through Age-Based Filtering. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2006, , .	0.0	7
23	A Load-Store Queue Design Based on Predictive State Filtering. Journal of Low Power Electronics, 2006, 2, 27-36.	0.6	5
24	A Power-Efficient and Scalable Load-Store Queue Design. Lecture Notes in Computer Science, 2005, , 1-9.	1.3	5
25	Customizing the branch predictor to reduce complexity and energy consumption. IEEE Micro, 2003, 23, 12-25.	1.8	23
26	Wavelet Transform for Large Scale Image Processing on Modern Microprocessors. Lecture Notes in Computer Science, 2003, , 549-562.	1.3	6
27	2-D Wavelet Transform Enhancement on General- Purpose Microprocessors: Memory Hierarchy and SIMD Parallelism Exploitation. Lecture Notes in Computer Science, 2002, , 9-21.	1.3	13