Bernabe Linares-Barranco

List of Publications by Year
in descending order

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162 papers	8,242 citations	87401 40 h-index	62345 84 g-index
164 all docs	164 docs citations	164 times ranked	5653 citing authors

#	Article	IF	Citations
1	Neuromorphic Context-Dependent Learning Framework With Fault-Tolerant Spike Routing. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 7126-7140.	7.2	101
2	How Frequency Injection Locking Can Train Oscillatory Neural Networks to Compute in Phase. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 1996-2009.	7.2	21
3	A Neuromorphic CMOS Circuit With Self-Repairing Capability. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 2246-2258.	7.2	7
4	2022 roadmap on neuromorphic computing and engineering. Neuromorphic Computing and Engineering, 2022, 2, 022501.	2.8	217
5	MemTorch: An Open-source Simulation Framework for Memristive Deep Learning Systems. Neurocomputing, 2022, 485, 124-133.	3.5	27
6	SAM: A Unified Self-Adaptive Multicompartmental Spiking Neuron Model for Learning With Working Memory. Frontiers in Neuroscience, 2022, 16, 850945.	1.4	47
7	Heterogeneous Ensemble-Based Spike-Driven Few-Shot Online Learning. Frontiers in Neuroscience, 2022, 16, .	1.4	72
8	Reliability Analysis of a Spiking Neural Network Hardware Accelerator. , 2022, , .		12
9	A CMOSâ€“memristor hybrid system for implementing stochastic binary spike timing-dependent plasticity. Philosophical Transactions Series A, Mathematical, Physical, and Engineering Sciences, 2022, 380, .	1.6	6
10	Neuromorphic Sensors, Vision. , 2022, , 2340-2344.		0
11	Neutron-Induced, Single-Event Effects on Neuromorphic Event-Based Vision Sensor: A First Step and Tools to Space Applications. IEEE Access, 2021, 9, 85748-85763.	2.6	9
12	Neuromorphic Low-Power Inference on Memristive Crossbars With On-Chip Offset Calibration. IEEE Access, 2021, 9, 38043-38061.	2.6	11
13	Neuron Fault Tolerance in Spiking Neural Networks. , 2021, , .		21
14	A Real-Time DSP-Based Biohybrid MEA System for Seizure Detection In Vitro. , 2021, , .		0
15	Novel programmable single pulse generator for producing pulse widths in different time scales. , 2021, , .		1
16	Hardware Implementation of Differential Oscillatory Neural Networks Using VO 2-Based Oscillators and Memristor-Bridge Circuits. Frontiers in Neuroscience, 2021, 15, 674567.	1.4	20
17	Baseline Features Extraction from Microelectrode Array Recordings in an in vitro model of Acute Seizures using Digital Signal Processing for Electronic Implementation. , 2021, , .		0
18	Digital Implementation of Oscillatory Neural Network for Image Recognition Applications. Frontiers in Neuroscience, 2021, 15, 713054.	1.4	15

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19	Insights Into the Dynamics of Coupled VO2 Oscillators for ONNs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3356-3360.	2.2	2
20	Event-driven implementation of deep spiking convolutional neural networks for supervised classification using the SpiNNaker neuromorphic platform. Neural Networks, 2020, 121, 319-328.	3.3	16
21	Sound Source Localization in Wide-Range Outdoor Environment Using Distributed Sensor Network. IEEE Sensors Journal, 2020, 20, 2234-2246.	2.4	20
22	Experimental Body-Input Three-Stage DC Offset Calibration Scheme for Memristive Crossbar. , 2020, , .		1
23	Lessons Learned the Hard Way. , 2020, , .		0
24	Hardware Implementation of Deep Network Accelerators Towards Healthcare and Biomedical Applications. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 1138-1159.	2.7	93
25	Implementation of a tunable spiking neuron for STDP with memristors in FDSOI 28nm. , 2020, , .		2
26	Enhanced Linearity in FD-SOI CMOS Body-Input Analog Circuits â€“ Application to Voltage-Controlled Ring Oscillators and Frequency-Based Î£Î” ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3297-3308.	3.5	6
27	System-level integration in neuromorphic co-processors. , 2020, , 479-497.		1
28	Introduction and Analysis of an Event-Based Sign Language Dataset. , 2020, , .		12
29	Auxiliary Pulse-Extender and Current-Attenuator Circuits for Flexible Interaction with Memristive Crossbars in SNNs. , 2020, , .		1
30	A Current-Attenuator for Performing Read Operation in Memristor-Based Spiking Neural Networks. , 2020, , .		0
31	Self-Testing Analog Spiking Neuron Circuit. , 2019, , .		9
32	Learning weights with STDP to build prototype images for classification. , 2019, , .		0
33	Asynchronous Spiking Neurons, the Natural Key to Exploit Temporal Sparsity. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 668-678.	2.7	15
34	Neuromorphic Spiking Neural Networks and Their Memristor-CMOS Hardware Implementations. Materials, 2019, 12, 2745.	1.3	71
35	A Neuromorphic Digital Circuit for Neuronal Information Encoding Using Astrocytic Calcium Oscillations. Frontiers in Neuroscience, 2019, 13, 998.	1.4	12
36	Bio-Inspired Evolutionary Model of Spiking Neural Networks in Ionic Liquid Space. Frontiers in Neuroscience, 2019, 13, 1085.	1.4	14

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37	Low-power hardware implementation of SNN with decision block for recognition tasks. , 2019, , .		5
38	Digital-Signal-Processor Realization of Izhikevich Neural Network for Real-Time Interaction with Electrophysiology Experiments. , 2019, , .		2
39	Spike-Timing-Dependent-Plasticity withÂMemristors. , 2019, , 429-467.		2
40	Digital Implementation of the Two-Compartmental Pinskyâ€“Rinzel Pyramidal Neuron Model. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 47-57.	2.7	19
41	Spiking Hough for Shape Recognition. Lecture Notes in Computer Science, 2018, , 425-432.	1.0	1
42	Memristors fire away. Nature Electronics, 2018, 1, 100-101.	13.1	12
43	Hybrid Neural Network, An Efficient Low-Power Digital Hardware Implementation of Event-based Artificial Neural Network. , 2018, , .		11
44	Event-Driven Stereo Visual Tracking Algorithm to Solve Object Occlusion. IEEE Transactions on Neural Networks and Learning Systems, 2018, 29, 4223-4237.	7.2	34
45	Scene Context Classification with Event-Driven Spiking Deep Neural Networks. , 2018, , .		2
46	Real-Time Temporal Frequency Detection in FPGA Using Event-Based Vision Sensor. , 2018, , .		4
47	On Practical Issues for Stochastic STDP Hardware With 1-bit Synaptic Weights. Frontiers in Neuroscience, 2018, 12, 665.	1.4	49
48	A Configurable Event-Driven Convolutional Node with Rate Saturation Mechanism for Modular ConvNet Systems Implementation. Frontiers in Neuroscience, 2018, 12, 63.	1.4	23
49	Calibration of offset via bulk for low-power HfO2 based 1T1R memristive crossbar read-out system. Microelectronic Engineering, 2018, 198, 35-47.	1.1	5
50	Performance Comparison of Time-Step-Driven versus Event-Driven Neural State Update Approaches in SpiNNaker. , 2018, , .		2
51	Active Perception With Dynamic Vision Sensors. Minimum Saccades With Optimum Recognition. IEEE Transactions on Biomedical Circuits and Systems, 2018, 12, 927-939.	2.7	16
52	A Hybrid CMOS-Memristor Neuromorphic Synapse. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 434-445.	2.7	108
53	On Multiple AER Handshaking Channels Over High-Speed Bit-Serial Bidirectional LVDS Links With Flow-Control and Clock-Correction on Commercial FPGAs for Scalable Neuromorphic Systems. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 1133-1147.	2.7	30
54	Bulk-based DC offset calibration for low-power memristor array read-out system. , 2017, , .		0

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55	An Event-Driven Classifier for Spiking Neural Networks Fed with Synthetic or Dynamic Vision Sensor Data. Frontiers in Neuroscience, 2017, 11, 350.	1.4	78
56	An Address Event Representation-Based Processing System for a Biped Robot. International Journal of Advanced Robotic Systems, 2016, 13, 39.	1.3	4
57	Fast Predictive Handshaking in Synchronous FPGAs for Fully Asynchronous Multisymbol Chip Links: Application to SpiNNaker 2-of-7 Links. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 763-767.	2.2	9
58	Plasticity in memristive devices for spiking neural networks. Frontiers in Neuroscience, 2015, 9, 51.	1.4	188
59	Generalized reconfigurable memristive dynamical system (MDS) for neuromorphic applications. Frontiers in Neuroscience, 2015, 9, 409.	1.4	3
60	Poker-DVS and MNIST-DVS. Their History, How They Were Made, and Other Details. Frontiers in Neuroscience, 2015, 9, 481.	1.4	88
61	Modeling and Experimental Demonstration of a Hopfield Network Analog-to-Digital Converter with Hybrid CMOS/Memristor Circuits. Frontiers in Neuroscience, 2015, 9, 488.	1.4	52
62	Feedforward Categorization on AER Motion Events Using Cortex-Like Features in a Spiking Neural Network. IEEE Transactions on Neural Networks and Learning Systems, 2015, 26, 1963-1978.	7.2	160
63	On the use of orientation filters for 3D reconstruction in event-driven stereo vision. Frontiers in Neuroscience, 2014, 8, 48.	1.4	25
64	Spike-Timing-Dependent-Plasticity in Hybrid Memristive-CMOS Spiking Neuromorphic Systems. , 2014, , 353-377.		1
65	Live demonstration: Event-driven sensing and processing for high-speed robotic vision. , 2014, , .		0
66	Event-driven sensing and processing for high-speed robotic vision. , 2014, , .		11
67	An AER handshake-less modular infrastructure PCB with x8 2.5Gbps LVDS serial links. , 2014, , .		23
68	Spiking neuro-fuzzy clustering system and its memristor crossbar based implementation. Microelectronics Journal, 2014, 45, 1450-1462.	1.1	9
69	Event-driven stereo vision with orientation filters. , 2014, , .		3
70	Retinomorphic Event-Based Vision Sensors: Bioinspired Cameras With Spiking Output. Proceedings of the IEEE, 2014, 102, 1470-1484.	16.4	270
71	A Proposal for Hybrid Memristor-CMOS Spiking Neuromorphic Learning Systems. IEEE Circuits and Systems Magazine, 2013, 13, 74-88.	2.6	56
72	A 128$,imes$128 1.5% Contrast Sensitivity 0.9% FPN 3 Âµs Latency 4 mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Preamplifiers. IEEE Journal of Solid-State Circuits, 2013, 48, 827-838.	3.5	268

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73	Integration of nanoscale memristor synapses in neuromorphic computing architectures. Nanotechnology, 2013, 24, 384010.	1.3	469
74	Mapping from Frame-Driven to Frame-Free Event-Driven Vision Systems by Low-Rate Rate Coding and Coincidence Processing–Application to Feedforward ConvNets. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2013, 35, 2706-2719.	9.7	230
75	Multicasting Mesh AER: A Scalable Assembly Approach for Reconfigurable Neuromorphic Structured AER Systems. Application to ConvNets. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 82-102.	2.7	83
76	A 1.5 ns OFF/ON Switching-Time Voltage-Mode LVDS Driver/Receiver Pair for Asynchronous AER Bit-Serial Chip Grid Links With Up to 40 Times Event-Rate Dependent Power Savings. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 722-731.	2.7	3
77	Improved contrast sensitivity DVS and its application to event-driven stereo vision. , 2013, , .		9
78	STDP and STDP variations with memristors for spiking neuromorphic learning systems. Frontiers in Neuroscience, 2013, 7, 2.	1.4	368
79	An Event-Driven Multi-Kernel Convolution Processor Module for Event-Driven Vision Sensors. IEEE Journal of Solid-State Circuits, 2012, 47, 504-517.	3.5	92
80	A Real-Time, Event-Driven Neuromorphic System for Goal-Directed Attentional Selection. Lecture Notes in Computer Science, 2012, , 226-233.	1.0	17
81	A <formula formulatype="inline"><tex Notation="TeX">${0.35}~mu{m m}$</tex></formula> Sub-ns Wake-up Time ON-OFF Switchable LVDS Driver-Receiver Chip I/O Pad Pair for Rate-Dependent Power Saving in AER Bit-Serial Links. IEEE Transactions on Biomedical Circuits and Systems, 2012, 6, 486-497.	2.7	14
82	Design of adaptive nano/CMOS neural architectures. , 2012, , .		12
83	Comparison between Frame-Constrained Fix-Pixel-Value and Frame-Free Spiking-Dynamic-Pixel ConvNets for Visual Processing. Frontiers in Neuroscience, 2012, 6, 32.	1.4	54
84	Efficient Feedforward Categorization of Objects and Human Postures with Address-Event Image Sensors. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2012, 34, 302-314.	9.7	93
85	A Memristive Nanoparticle/Organic Hybrid Synapstor for Neuroinspired Computing. Advanced Functional Materials, 2012, 22, 609-616.	7.8	163
86	A 32$,imes,$32 Pixel Convolution Processor Chip for Address Event Vision Sensors With 155 ns Event Latency and 20 Meps Throughput. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 777-790.	3.5	47
87	Neuromorphic Silicon Neuron Circuits. Frontiers in Neuroscience, 2011, 5, 73.	1.4	1,004
88	A 3.6 mus Latency Asynchronous Frame-Free Event-Driven Dynamic-Vision-Sensor. IEEE Journal of Solid-State Circuits, 2011, 46, 1443-1455.	3.5	196
89	An Instant-Startup Jitter-Tolerant Manchester-Encoding Serializer/Deserializer Scheme for Event-Driven Bit-Serial LVDS Interchip AER Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2647-2660.	3.5	17
90	On Spike-Timing-Dependent-Plasticity, Memristive Devices, and Building a Self-Learning Visual Cortex. Frontiers in Neuroscience, 2011, 5, 26.	1.4	364

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91	Confession session: Learning from others mistakes. , 2011, , .		2
92	Voltage mode driver for low power transmission of high speed serial AER Links. , 2011, , .		4
93	Performance Study of Software AER-Based Convolutions on a Parallel Supercomputer. Lecture Notes in Computer Science, 2011, , 141-148.	1.0	2
94	On scalable spiking convnet hardware for cortex-like visual sensory processing systems. , 2010, , .		6
95	Activity-driven, event-based vision sensors. , 2010, , .		157
96	A signed spatial contrast event spike retina chip. , 2010, , .		5
97	Spike-Based Convolutional Network for Real-Time Processing. , 2010, , .		13
98	On neuromorphic spiking architectures for asynchronous STDP memristive systems. , 2010, , .		46
99	Fast Vision Through Frameless Event-Based Sensing and Convolutional Processing: Application to Texture Recognition. IEEE Transactions on Neural Networks, 2010, 21, 609-620.	4.8	32
100	A Five-Decade Dynamic-Range Ambient-Light-Independent Calibrated Signed-Spatial-Contrast AER Retina With 0.1-ms Latency and Optional Time-to-First-Spike Mode. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 2632-2643.	3.5	34
101	Neocortical frame-free vision sensing and processing through scalable Spiking ConvNet hardware. , 2010, , .		0
102	OTA-C oscillator with low frequency variations for on-chip clock generation in serial LVDS-AER links. , 2009, , .		2
103	A mismatch calibrated bipolar spatial contrast AER retina with adjustable contrast threshold. , 2009, , .		2
104	CAVIAR: A 45k Neuron, 5M Synapse, 12G Connects/s AER Hardware Sensoryâ€“Processingâ€“ Learningâ€“Actuating System for High-Speed Visual Object Recognition and Tracking. IEEE Transactions on Neural Networks, 2009, 20, 1417-1438.	4.8	285
105	A weak-to-strong inversion mismatch model for analog circuit design. Analog Integrated Circuits and Signal Processing, 2009, 59, 325-340.	0.9	3
106	Advanced Vision Processing Systems: Spike-Based Simulation and Processing. Lecture Notes in Computer Science, 2009, , 640-651.	1.0	4
107	A Calibration Technique for Very Low Current and Compact Tunable Neuromorphic Cells: Application to 5-bit 20-nA DACs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 522-526.	2.2	16
108	On Real-Time AER 2-D Convolutions Hardware for Neuromorphic Spike-Based Cortical Processing. IEEE Transactions on Neural Networks, 2008, 19, 1196-1219.	4.8	65

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109	Compact calibration circuit for large neuromorphic arrays. , 2008, , .		0
110	Fully digital AER convolution chip for vision processing. , 2008, , .		9
111	High-speed character recognition system based on a complex hierarchical AER architecture. , 2008, , .		4
112	LVDS interface for AER links with burst mode operation capability. , 2008, , .		6
113	Event based vision sensing and processing. , 2008, , .		1
114	On an Efficient CAD Implementation of the Distance Term in Pelgrom's Mismatch Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1534-1538.	1.9	8
115	The Stochastic I-Pot: A Circuit Block for Programming Bias Currents. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 760-764.	2.2	20
116	A Spatial Contrast Retina With On-Chip Calibration for Neuromorphic Spike-Based AER Vision Systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 1444-1458.	0.1	90
117	Inter-spike-intervals analysis of AER Poisson-like generator hardware. Neurocomputing, 2007, 70, 2692-2700.	3.5	15
118	A Neuromorphic Cortical-Layer Microchip for Spike-Based Event Processing Vision Systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 2548-2566.	0.1	88
119	On algorithmic rate-coded AER generation. IEEE Transactions on Neural Networks, 2006, 17, 771-788.	4.8	60
120	A Low-Power Current Mode Fuzzy-ART Cell. IEEE Transactions on Neural Networks, 2006, 17, 1666-1673.	4.8	6
121	A calibration scheme for subthreshold current mode circuits. , 2005, , .		0
122	AER synthetic generation in hardware for bio-inspired spiking systems. , 2005, , .		0
123	A digital pixel cell for address event representation image convolution processing. , 2005, , .		2
124	Event generators for address event representation transmitters. , 2005, 5839, 148.		4
125	<title>A mismatch characterization and simulation environment for weak-to-strong inversion CMOS transistors</title>. , 2005, , .		1
126	A Precise 90<tex>^circ</tex>Quadrature OTA-C Oscillator Tunable in the 50â€“130-MHz Range. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2004, 51, 649-663.	0.1	32

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127	Current Mode Techniques for Sub-pico-Ampere Circuit Design. Analog Integrated Circuits and Signal Processing, 2004, 38, 103-119.	0.9	30
128	Precise 90Â° quadrature current-controlled oscillator tunable between 50â€“130â€…MHz. Electronics Letters, 2003, 39, 823.	0.5	0
129	On the design and characterization of femtoampere current-mode circuits. IEEE Journal of Solid-State Circuits, 2003, 38, 1353-1363.	3.5	161
130	Log-domain implementation of complex dynamics reaction-diffusion neural networks. IEEE Transactions on Neural Networks, 2003, 14, 1337-1355.	4.8	40
131	Compact low-power calibration mini-DACs for neural arrays with programmable weights. IEEE Transactions on Neural Networks, 2003, 14, 1207-1216.	4.8	44
132	Guest editorial - Special issue on neural networks hardware implementations. IEEE Transactions on Neural Networks, 2003, 14, 976-979.	4.8	17
133	Current-mode fully-programmable piece-wise-linear block for neuro-fuzzy applications. Electronics Letters, 2002, 38, 1165.	0.5	14
134	A Programmable VLSI Filter Architecture for Application in Real-Time Vision Processing Systems. International Journal of Neural Systems, 2000, 10, 179-190.	3.2	4
135	A new five-parameter MOS transistor mismatch model. IEEE Electron Device Letters, 2000, 21, 37-39.	2.2	24
136	Very wide range tunable CMOS/bipolar current mirrors with voltage clamped input. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1999, 46, 1398-1407.	0.1	41
137	Systematic Width-and-Length Dependent CMOS Transistor Mismatch Characterization and Simulation. Analog Integrated Circuits and Signal Processing, 1999, 21, 271-296.	0.9	42
138	AER image filtering architecture for vision-processing systems. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1999, 46, 1064-1071.	0.1	80
139	A general translinear principle for subthreshold MOS transistors. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1999, 46, 607-616.	0.1	69
140	Bipolar/CMOS current-source flip-flop for application in neuro-fuzzy systems. Electronics Letters, 1999, 35, 1326.	0.5	2
141	Adaptive resonance theory microchips. Lecture Notes in Computer Science, 1999, , 737-746.	1.0	8
142	A high-precision current-mode WTA-MAX circuit with multichip capability. IEEE Journal of Solid-State Circuits, 1998, 33, 280-286.	3.5	44
143	Adaptive Resonance Theory Microchips. , 1998, , .		31
144	7-decade tuning range CMOS OTA-C sinusoidal VCO. Electronics Letters, 1998, 34, 1621.	0.5	16

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145	An ART1 microchip and its use in multi-ART1 systems. IEEE Transactions on Neural Networks, 1997, 8, 1184-1194.	4.8	17
146	A real-time clustering microchip neural engine. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 1996, 4, 195-209.	2.1	23
147	A Modified ART 1 Algorithm more Suitable for VLSI Implementations. Neural Networks, 1996, 9, 1025-1043.	3.3	26
148	A modular current-mode high-precision winner-take-all circuit. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1995, 42, 132-134.	2.3	42
149	CMOS Analog Neural Network Systems Based on Oscillatory Neurons. , 1994, , 199-247.		1
150	The active-input regulated-cascode current mirror. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 1994, 41, 464-467.	0.1	76
151	A CMOS analog adaptive BAM with on-chip learning and weight refreshing. IEEE Transactions on Neural Networks, 1993, 4, 445-455.	4.8	49
152	A modular T-mode design approach for analog neural network hardware implementations. IEEE Journal of Solid-State Circuits, 1992, 27, 701-713.	3.5	32
153	CMOS OTA-C high-frequency sinusoidal oscillators. IEEE Journal of Solid-State Circuits, 1991, 26, 160-165.	3.5	55
154	A CMOS implementation of FitzHugh-Nagumo neuron model. IEEE Journal of Solid-State Circuits, 1991, 26, 956-965.	3.5	114
155	On the design of voltage-controlled sinusoidal oscillators using OTAs. IEEE Transactions on Circuits and Systems, 1990, 37, 198-211.	0.9	111
156	A programmable neural oscillator cell. IEEE Transactions on Circuits and Systems, 1989, 36, 756-761.	0.9	22
157	Operational transconductance amplifier-based nonlinear function syntheses. IEEE Journal of Solid-State Circuits, 1989, 24, 1576-1586.	3.5	138
158	CMOS transistor mismatch model valid from weak to strong inversion. , 0, , .		23
159	MOSFET mismatch in weak/moderate inversion: model needs and implications for analog design. , 0, , .		12
160	A Bio-inspired Event-Based Real-Time Image Processor. , 0, , .		0
161	Memristance can explain Spike-Time-Dependent-Plasticity in Neural Synapses. Nature Precedings, 0, , .	0.1	128
162	SL-Animals-DVS: event-driven sign language animals dataset. Pattern Analysis and Applications, 0, , 1.	3.1	5