Jen-Wei Hsieh

List of Publications by Year
in descending order

19	200	1684188 5	1199594 12
papers	citations	h-index	g-index

19	19	19	158
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Alternative Encoding: A Two-Step Transition Reduction Scheme for MLC STT-RAM Cache. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2753-2757.	2.7	1
2	EMT: Elegantly Measured Tanner for Key-Value Store on SSD. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 91-103.	2.7	1
3	Differential Evolution Algorithm With Asymmetric Coding for Solving the Reliability Problem of 3D-TLC CT Flash-Memory Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2863-2876.	2.7	2
4	TSE: Two-Step Elimination for MLC STT-RAM Last-Level Cache. IEEE Transactions on Computers, 2021, 70, 1498-1510.	3.4	5
5	A Management Scheme of Multi-Level Retention-Time Queues for Improving the Endurance of Flash-Memory Storage Devices. IEEE Transactions on Computers, 2020, 69, 549-562.	3.4	4
6	Revive Bad Flash-Memory Pages by HLC Scheme. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 860-873.	2.7	3
7	Retention-Time Relaxation Scheme for MLC Flash-Memory Storage Systems. , 2018, , .		2
8	DCCS: Double Circular Caching Scheme for DRAM/PRAM Hybrid Cache. IEEE Transactions on Computers, 2015, 64, 3115-3127.	3.4	2
9	Adaptive ECC Scheme for Hybrid SSDâ€™s. IEEE Transactions on Computers, 2015, 64, 3348-3361.	3.4	15
10	Block-Based Multi-Version B$^+$-Tree for Flash-Based Embedded Database Systems. IEEE Transactions on Computers, 2015, 64, 925-940.	3.4	12
11	Multi-Channel Architecture-Based FTL for Reliable and High-Performance SSD. IEEE Transactions on Computers, 2014, 63, 3079-3091.	3.4	12
12	Garbage collection for multi-version index on flash memory. , 2014, , .		0
13	Garbage collection for multi-version index on flash memory. , 2014, , .		0
14	VAST: Virtually Associative Sector Translation for MLC Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1137-1150.	2.7	3
15	Double Circular Caching Scheme for DRAM/PRAM Hybrid Cache. , 2012, , .		6
16	An enhanced leakage-aware scheduler for dynamically reconfigurable FPGAs. , 2011, , .		6
17	Set-based management scheme for MLC flash memory storage system. , 2011, , .		1
18	Improving Flash Wear-Leveling by Proactively Moving Static Data. IEEE Transactions on Computers, 2010, 59, 53-65.	3.4	101

#	Article	IF	Citations
19	The Behavior Analysis of Flash-Memory Storage Systems. , 2008, , .		24