

Jen-Wei Hsieh

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/3259192/publications.pdf>

Version: 2024-02-01

19
papers

200
citations

1684188

5
h-index

1199594

12
g-index

19
all docs

19
docs citations

19
times ranked

158
citing authors

#	ARTICLE	IF	CITATIONS
1	Improving Flash Wear-Leveling by Proactively Moving Static Data. IEEE Transactions on Computers, 2010, 59, 53-65.	3.4	101
2	The Behavior Analysis of Flash-Memory Storage Systems. , 2008, , .		24
3	Adaptive ECC Scheme for Hybrid SSDs. IEEE Transactions on Computers, 2015, 64, 3348-3361.	3.4	15
4	Multi-Channel Architecture-Based FTL for Reliable and High-Performance SSD. IEEE Transactions on Computers, 2014, 63, 3079-3091.	3.4	12
5	Block-Based Multi-Version B+ -Tree for Flash-Based Embedded Database Systems. IEEE Transactions on Computers, 2015, 64, 925-940.	3.4	12
6	An enhanced leakage-aware scheduler for dynamically reconfigurable FPGAs. , 2011, , .		6
7	Double Circular Caching Scheme for DRAM/PRAM Hybrid Cache. , 2012, , .		6
8	TSE: Two-Step Elimination for MLC STT-RAM Last-Level Cache. IEEE Transactions on Computers, 2021, 70, 1498-1510.	3.4	5
9	A Management Scheme of Multi-Level Retention-Time Queues for Improving the Endurance of Flash-Memory Storage Devices. IEEE Transactions on Computers, 2020, 69, 549-562.	3.4	4
10	VAST: Virtually Associative Sector Translation for MLC Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1137-1150.	2.7	3
11	Revive Bad Flash-Memory Pages by HLC Scheme. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 860-873.	2.7	3
12	DCCS: Double Circular Caching Scheme for DRAM/PRAM Hybrid Cache. IEEE Transactions on Computers, 2015, 64, 3115-3127.	3.4	2
13	Retention-Time Relaxation Scheme for MLC Flash-Memory Storage Systems. , 2018, , .		2
14	Differential Evolution Algorithm With Asymmetric Coding for Solving the Reliability Problem of 3D-TLC CT Flash-Memory Storage Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2863-2876.	2.7	2
15	Set-based management scheme for MLC flash memory storage system. , 2011, , .		1
16	Alternative Encoding: A Two-Step Transition Reduction Scheme for MLC STT-RAM Cache. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2753-2757.	2.7	1
17	EMT: Elegantly Measured Tanner for Key-Value Store on SSD. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 91-103.	2.7	1
18	Garbage collection for multi-version index on flash memory. , 2014, , .		0

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19	Garbage collection for multi-version index on flash memory. , 2014, , .		0