Nuno Horta

List of Publications by Year
in descending order

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196 papers	1,837 citations	361045 20 h-index	395343 33 g-index
249 all docs	249 docs citations	249 times ranked	991 citing authors

#	Article	IF	Citations
1	DeepPlacer: A custom integrated OpAmp placement tool using deep models. Applied Soft Computing Journal, 2022, 115, 108188.	4.1	6
2	Radiation-Hardened Bandgap Voltage and Current Reference for Space Applications with 2.38 ppm/Â°C Temperature Coefficient. , 2022, , .		1
3	A Machine Learning based Pairs Trading Investment Strategy. SpringerBriefs in Applied Sciences and Technology, 2021, , .	0.2	3
4	Shortening the gap between pre- and post-layout analog IC performance by reducing the LDE-induced variations with multi-objective simulated quantum annealing. Engineering Applications of Artificial Intelligence, 2021, 98, 104102.	4.3	9
5	Tunable Low-Power Low-Noise Amplifier for Healthcare Applications. SpringerBriefs in Applied Sciences and Technology, 2021, , .	0.2	0
6	Background and State-of-the-Art. SpringerBriefs in Applied Sciences and Technology, 2021, , 7-35.	0.2	0
7	Hierarchical Yield-Aware Synthesis Methodology Covering Device-, Circuit-, and System-Level for Radiofrequency ICs. IEEE Access, 2021, 9, 124152-124164.	2.6	4
8	Pairs Tradingâ€"Background and Related Work. SpringerBriefs in Applied Sciences and Technology, 2021, , 7-19.	0.2	0
9	Proposed Trading Model. SpringerBriefs in Applied Sciences and Technology, 2021, , 37-49.	0.2	0
10	Proposed Pairs Selection Framework. SpringerBriefs in Applied Sciences and Technology, 2021, , 21-35.	0.2	0
11	FUZYE: A Fuzzy ${c}$ -Means Analog IC Yield Optimization Using Evolutionary-Based Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 1-13.	1.9	16
12	A Folded Voltage-Combiners Biased Amplifier for Low Voltage and High Energy-Efficiency Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 230-234.	2.2	7
13	Optimizing earthquake design of reinforced concrete bridge infrastructures based on evolutionary computation techniques. Structural and Multidisciplinary Optimization, 2020, 61, 1087-1105.	1.7	8
14	A new family of CMOS inverter-based OTAs for biomedical and healthcare applications. The Integration VLSI Journal, 2020, 71, 38-48.	1.3	6
15	Sub-Î¼W Tow-Thomas based biquad filter with improved gain for biomedical applications. Microelectronics Journal, 2020, 95, 104675.	1.1	12
16	Using Artificial Neural Networks for Analog Integrated Circuit Design Automation. SpringerBriefs in Applied Sciences and Technology, 2020, , .	0.2	6
17	Semi-Supervised Artificial Neural Networks towards Analog IC Placement Recommender. , 2020, , .		13
18	Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3965-3977.	3.5	22

#	Article	IF	Citations
19	Enhancing a Pairs Trading strategy with the application of Machine Learning. Expert Systems With Applications, 2020, 158, 113490.	4.4	18
20	Ready-to-Fabricate RF Circuit Synthesis Using a Layout- and Variability-Aware Optimization-Based Methodology. IEEE Access, 2020, 8, 51601-51609.	2.6	7
21	Analog IC Placement Generation via Neural Networks from Unlabeled Data. SpringerBriefs in Applied Sciences and Technology, 2020, , .	0.2	0
22	Overview of Artificial Neural Networks. SpringerBriefs in Applied Sciences and Technology, 2020, , 21-44.	0.2	14
23	Artificial Neural Network Overview. SpringerBriefs in Applied Sciences and Technology, 2020, , 7-24.	0.2	2
24	ANNs as an Alternative for Automatic Analog IC Placement. SpringerBriefs in Applied Sciences and Technology, 2020, , 67-101.	0.2	0
25	ANN Models for Analog Placement Automation. SpringerBriefs in Applied Sciences and Technology, 2020, , 39-58.	0.2	0
26	Two-Step RF IC Block Synthesis With Preoptimized Inductors and Full Layout Generation In-the-Loop. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 989-1002.	1.9	29
27	Using EDA Tools to Push the Performance Boundaries of an Ultralow-Power IoT-VCO at 65nm. , 2019, , .		0
28	A Low Noise CMOS Inverter-Based OTA for and Healthcare Signal Receivers. , 2019, , .		0
29	On the Exploration of Design Tradeoffs in Analog IC Placement with Layout-dependent Effects. , 2019, , .		7
30	Multi-objective framework for cost-effective OTN switch placement using NSGA-II with embedded domain knowledge. Applied Soft Computing Journal, 2019, 83, 105608.	4.1	12
31	A 302 uW CMOS Temperature Sensor to compensate frequency drift for an oscillator. , 2019, , .		0
32	Artificial Neural Networks as an Alternative for Automatic Analog IC Placement. , 2019, , .		14
33	Using Polynomial Regression and Artificial Neural Networks for Reusable Analog IC Sizing. , 2019, , .		16
34	Hard and Soft Constraints for Multi-objective Analog IC Sizing Optimization. , 2019, , .		1
35	Synthesis of mm-Wave circuits using-EM-simulated passive structure libraries. , 2019, , .		1
36	Nonlinear A/D Converters. Lecture Notes in Electrical Engineering, 2019, , 11-36.	0.3	0

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37	Circuit and Layout Level Validation. Lecture Notes in Electrical Engineering, 2019, , 75-94.	0.3	0
38	Evaluation of the Prototype. Lecture Notes in Electrical Engineering, 2019, , 95-109.	0.3	0
39	Future Work and Conclusions. Lecture Notes in Electrical Engineering, 2019, , 111-117.	0.3	0
40	Many-Objective Sizing Optimization of a Class-C/D VCO for Ultralow-Power IoT and Ultralow-Phase-Noise Cellular Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 69-82.	2.1	24
41	Enhanced systematic design of a voltage controlled oscillator using a two-step optimization methodology. The Integration VLSI Journal, 2018, 63, 351-361.	1.3	17
42	SIR/GA Approach. SpringerBriefs in Applied Sciences and Technology, 2018, , 29-44.	0.2	0
43	Combining Support Vector Machine with Genetic Algorithms to optimize investments in Forex markets with high leverage. Applied Soft Computing Journal, 2018, 64, 596-613.	4.1	42
44	Enhanced analog and RF IC sizing methodology using PCA and NSGA-II optimization kernel. , 2018, , .		5
45	Parallel SAX/GA for financial pattern matching using NVIDIAâ€™s GPU. Expert Systems With Applications, 2018, 105, 77-88.	4.4	5
46	Single-Stage OTA Biased by Voltage-Combiners With Enhanced Performance Using Current Starving. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1599-1603.	2.2	9
47	Centralized Unmanned Aerial Vehicle Mesh Network Placement Scheme: A Multi-Objective Evolutionary Algorithm Approach. Sensors, 2018, 18, 4387.	2.1	28
48	A 20 DB Gain Two-Stage Low-Noise Amplifier with High Yield for 5 GHz Applications. , 2018, , .		1
49	An Integrated LC Oscillator with Self Compensation for Frequency Drift and PVT Corners Variations. , 2018, , .		1
50	Handling the Effects of Variability and Layout Parasitics in the Automatic Synthesis of LNAs. , 2018, , .		3
51	Reinforcement learning applied to Forex trading. Applied Soft Computing Journal, 2018, 73, 783-794.	4.1	60
52	Analog active filter design using a multi objective genetic algorithm. AEU - International Journal of Electronics and Communications, 2018, 93, 83-94.	1.7	16
53	Second-order compensation BGR with low TC and high performance for space applications. The Integration VLSI Journal, 2018, 63, 256-265.	1.3	3
54	11.7b Time-To-Digital Converter with 0.82ps resolution in 130nm CMOS Technology. , 2018, , .		4

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55	On the Exploration of Promising Analog IC Designs via Artificial Neural Networks. , 2018, , .		14
56	Design and Optimization of a Class-C/D VCO for Ultra-Low-Power IoT and Cellular Applications. , 2018, , .		0
57	GPU-Accelerated SAX/GA. SpringerBriefs in Applied Sciences and Technology, 2018, , 45-66.	0.2	0
58	State-of-the-Art in Pattern Recognition Techniques. SpringerBriefs in Applied Sciences and Technology, 2018, , 21-32.	0.2	0
59	Efficient yield optimization method using a variable K-Means algorithm for analog IC sizing. , 2017, , .		11
60	Stochastic-based placement template generator for analog IC layout-aware synthesis. The Integration VLSI Journal, 2017, 58, 485-495.	1.3	8
61	Layout-aware challenges and a solution for the automatic synthesis of radio-frequency IC blocks. , 2017, , .		0
62	Systematic design of a voltage controlled oscillator using a layout-aware approach. , 2017, , .		0
63	New mapping strategies for pre-optimized inductor sets in bottom-up RF IC sizing optimization. , 2017, , .		3
64	Using sentiment from Twitter optimized by Genetic Algorithms to predict the stock market. , 2017, , .		9
65	A dynamic voltage-combiners biased OTA for low-power and high-speed SC circuits. , 2017, , .		0
66	Automatic technology migration of analog IC designs using generic cell libraries. , 2017, , .		3
67	Empirical-Based Parasitic Extractor. , 2017, , 137-155.		0
68	Layout-Aware Circuit Sizing. , 2017, , 121-146.		0
69	Automatic Analog IC Sizing and Optimization Constrained with PVT Corners and Layout Effects. , 2017, , .		30
70	Experimental Results. , 2017, , 157-198.		0
71	State-of-the-Art on Analog Layout Automation. , 2017, , 11-41.		1
72	Template-Based Placer. , 2017, , 61-81.		0

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73	AIDA-L: Architecture and Integration. , 2017, , 43-59.		0
74	Analog Integrated Circuit Design Automation. , 2017, , .		13
75	Fully-Automatic Router. , 2017, , 105-136.		0
76	Company event popularity for financial markets using Twitter and sentiment analysis. Expert Systems With Applications, 2017, 71, 111-124.	4.4	84
77	Design of a BGR Suitable for the Space Industry with Performance of 1.25 V with 0.758 ppm/Â°C TC from -55Â° to 125Â°C. , 2017, , .		2
78	Multi-objective Optimization Kernel. , 2017, , 63-86.		0
79	AIDA-C Layout-Aware Circuit Sizing Results. , 2017, , 147-175.		0
80	Previous Works on Automatic Analog IC Sizing. , 2017, , 13-37.		0
81	Optimization-Based Placer. , 2017, , 83-104.		0
82	AIDA-C Architecture. , 2017, , 39-61.		0
83	On-the-fly exploration of placement templates for analog IC layout-aware sizing methodologies. , 2016, , .		2
84	Design of a radiation-hardened curvature compensated bandgap reference circuit. , 2016, , .		2
85	AIDA: Layout-aware analog circuit-level sizing with in-loop layout generation. The Integration VLSI Journal, 2016, 55, 316-329.	1.3	49
86	SCALES: A high speed simulator tool for pipeline A/D converters. , 2016, , .		0
87	An 8bit logarithmic AD converter Using cross-coupled inverters and a time-to-digital converter. , 2016, , .		0
88	Current-flow and current-density-aware multi-objective optimization of analog IC placement. The Integration VLSI Journal, 2016, 55, 295-306.	1.3	21
89	Automated analog IC design constraints generation for a layout-aware sizing approach. , 2016, , .		2
90	Yield optimization using k-means clustering algorithm to reduce Monte Carlo simulations. , 2016, , .		7

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91	Combining rules between PIPs and SAX to identify patterns in financial markets. Expert Systems With Applications, 2016, 65, 242-254.	4.4	13
92	Design and application of a CMOS active inductor at Ku band based on a multi-objective optimizer. The Integration VLSI Journal, 2016, 55, 330-340.	1.3	5
93	A Novel Approach for Optimization in Dynamic Environments Based on Modified Artificial Fish Swarm Algorithm. International Journal of Computational Intelligence and Applications, 2016, 15, 1650010.	0.6	19
94	Logarithmic AD Converter With Selectable Transfer Characteristic. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 234-238.	2.2	2
95	Multi-objective kernel mapping and scheduling for morphable many-core architectures. Expert Systems With Applications, 2016, 45, 385-399.	4.4	1
96	Automatic synthesis of RF front-end blocks using multi-objective evolutionary techniques. The Integration VLSI Journal, 2016, 52, 243-252.	1.3	27
97	Design Automation Tasks Scheduling for Enhanced Parallel Execution of a State-of-the-Art Layout-Aware Sizing Approach. , 2016, , .		2
98	System Architecture. SpringerBriefs in Applied Sciences and Technology, 2016, , 39-56.	0.2	0
99	Multi-objective Optimization. SpringerBriefs in Applied Sciences and Technology, 2016, , 57-72.	0.2	1
100	Embedding Fault List Compression techniques in a design automation framework for analog and Mixed-Signal structural testing. , 2015, , .		6
101	Analog IC placement using absolute coordinates and a hierarchical combination of Pareto optimal fronts. , 2015, , .		2
102	AIDA-PEx: Accurate parasitic extraction for layout-aware analog integrated circuit sizing. , 2015, , .		7
103	Extraction and application of wiring symmetry rules to route analog multiport terminals. , 2015, , .		6
104	Exploring design tradeoffs in analog IC placement with current-flow & current-density considerations. , 2015, , .		2
105	A multi-objective routing algorithm for Wireless Multimedia Sensor Networks. Applied Soft Computing Journal, 2015, 30, 104-112.	4.1	46
106	AIDA-CMK: Multi-Algorithm Optimization Kernel Applied to Analog IC Sizing. SpringerBriefs in Applied Sciences and Technology, 2015, , .	0.2	6
107	Boosting Trading Strategies performance using VIX indicator together with a dual-objective Evolutionary Computation optimizer. Expert Systems With Applications, 2015, 42, 6699-6716.	4.4	14
108	A multi-objective model for scheduling of short-term incentive-based demand response programs offered by electricity retailers. Applied Energy, 2015, 151, 102-118.	5.1	111

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109	Grounded active inductors design optimization for fQmax = 14.2GHz using a 130 nm CMOS technology. , 2015, , .		7
110	Scheduling evaluation tasks for increased efficiency of parallel analog IC synthesis. , 2015, , .		0
111	AIDA: Robust layout-aware synthesis of analog ICs including sizing and layout generation. , 2015, , .		24
112	Thermal-aware floorplanning and layout generation of MOSFET power stages. , 2015, , .		0
113	Developing Multi-Time Frame Trading Rules with a Trend Following Strategy, using GA. , 2015, , .		4
114	Automatic Layout Optimizations for Integrated MOSFET Power Stages. , 2015, , 147-175.		0
115	A voltage-combiners-biased amplifier with enhanced gain and speed using current starving. , 2015, , .		3
116	Multi-objective optimization of analog integrated circuit placement hierarchy in absolute coordinates. Expert Systems With Applications, 2015, 42, 9137-9151.	4.4	26
117	Floorplan-aware analog IC sizing and optimization based on topological constraints. The Integration VLSI Journal, 2015, 48, 183-197.	1.3	26
118	A hybrid approach to portfolio composition based on fundamental and technical indicators. Expert Systems With Applications, 2015, 42, 2036-2048.	4.4	38
119	Solving a Capacitated Exam Timetabling Problem Instance Using a Bi-objective NSGA-II. Studies in Computational Intelligence, 2015, , 115-129.	0.7	2
120	Enhancing an Automatic Analog IC Design Flow by Using a Technology-Independent Module Generator. Advances in Computer and Electrical Engineering Book Series, 2015, , 102-133.	0.2	1
121	Layout-Aware Sizing of Analog ICs using Floorplan & Routing Estimates for Parasitic Extraction. , 2015, , .		24
122	Synthesis of LC-Oscillators Using Rival Multi-Objective Multi-Constraint Optimization Kernels. Advances in Computer and Electrical Engineering Book Series, 2015, , 1-27.	0.2	3
123	AIDA-CMK: AIDA-C with MOO Framework. SpringerBriefs in Applied Sciences and Technology, 2015, , 17-31.	0.2	0
124	Previous Works on Automated Analog IC Sizing. SpringerBriefs in Applied Sciences and Technology, 2015, , 7-16.	0.2	2
125	Electromigration-aware and IR-Drop avoidance routing in analog multiport terminal structures. , 2014, , .		6
126	A cascode-free single-stage amplifier using a fully-differential folded voltage-combiner. , 2014, , .		4

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127	Logarithmic AD conversion using latched comparators and a time-to-digital converter. , 2014, , .		1
128	Automatic layout generation of power MOSFET transistors in bulk CMOS. , 2014, , .		1
129	A rad-hard DC-DC converter controller. , 2014, , .		5
130	Routing analog ICs using a multi-objective multi-constraint evolutionary approach. Analog Integrated Circuits and Signal Processing, 2014, 78, 123-135.	0.9	10
131	Electromigration-aware analog Router with multilayer multiport terminal structures. The Integration VLSI Journal, 2014, 47, 532-547.	1.3	21
132	A survey on nonlinear analog-to-digital converters. The Integration VLSI Journal, 2014, 47, 12-22.	1.3	19
133	LC-VCO automatic synthesis using multi-objective evolutionary techniques. , 2014, , .		18
134	Portfolio optimization using fundamental indicators based on multi-objective EA. , 2014, , .		4
135	Electromigration-aware and IR-Drop avoidance routing in analog multiport terminal structures. , 2014, , .		4
136	State-of-the-Art on Automatic Analog IC Sizing. SpringerBriefs in Applied Sciences and Technology, 2014, , 7-22.	0.2	5
137	Enhanced AIDAâ€™s Circuit-Level Optimization Kernel. SpringerBriefs in Applied Sciences and Technology, 2014, , 35-50.	0.2	0
138	A SAX-GA approach to evolve investment strategies on financial markets based on pattern discovery techniques. Expert Systems With Applications, 2013, 40, 1579-1590.	4.4	29
139	Multi-dimensional pattern discovery in financial time series using sax-ga with extended robustness. , 2013, , .		7
140	LAYGEN Iiâ€”Automatic Layout Generation of Analog Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1641-1654.	1.9	75
141	Optimizing investment strategies based on companies earnings using genetic algorithms. , 2013, , .		0
142	Multi-port multi-terminal analog router based on an evolutionary optimization kernel. , 2013, , .		1
143	A new metaheuristc combining gradient models with NSGA-II to enhance analog IC synthesis. , 2013, , .		3
144	Single-stage amplifiers with gain enhancement and improved energy-efficiency employing voltage-combiners. , 2013, , .		20

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145	Analog Circuit Design Based on Robust POFs Using an Enhanced MOEA with SVM Models. Lecture Notes in Electrical Engineering, 2013, , 149-167.	0.3	8
146	GENOM-POF. , 2012, , .		40
147	An evolutionary approach to define investment strategies based on macroeconomic indicators and VIX data. , 2012, , .		0
148	Automated passive filter design using multi-objective genetic algorithms with variable parameters. , 2012, , .		0
149	LAYGEN II. , 2012, , .		15
150	A new SAX-GA methodology applied to investment strategies optimization. , 2012, , .		10
151	Automatic topology selection and sizing of class-D loop-filters for minimizing distortion based on an evolutionary optimization kernel. Analog Integrated Circuits and Signal Processing, 2012, 73, 21-32.	0.9	0
152	AIDA: Automated analog IC design flow from circuit level to layout. , 2012, , .		33
153	SCALES - A behavioral simulator for pipelined analog-to-digital converter design. , 2012, , .		1
154	Multi-objective multi-constraint routing of analog ICs using a Modified NSGA-II Approach. , 2012, , .		6
155	Overcurrent detection circuit for integrated class-D amplifiers. , 2011, , .		1
156	Trading with optimized uptrend and downtrend pattern templates using a genetic algorithm kernel. , 2011, , .		14
157	Applying a GA kernel on optimizing technical analysis rules for stock picking and portfolio composition. Expert Systems With Applications, 2011, , .	4.4	24
158	Fitness function evaluation for MA trading strategies based on genetic algorithms. , 2011, , .		5
159	Optimal OpAmp sizing based on a fuzzy-genetic kernel. , 2011, , .		0
160	Analog circuits optimization based on evolutionary computation techniques. The Integration VLSI Journal, 2010, 43, 136-155.	1.3	86
161	Trading in financial markets using pattern recognition optimized by genetic algorithms. , 2010, , .		7
162	State-of-the-Art on Analog Design Automation. Studies in Computational Intelligence, 2010, , 19-47.	0.7	3

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163	Optimization of Analog Circuits and Systems - Applications. Studies in Computational Intelligence, 2010, , 139-186.	0.7	2
164	Automatic topology selection and sizing of Class-D loop-filters for minimizing distortion. , 2010, , .		1
165	Enhanced Techniques for Analog Circuits Design Using SVM Models. Studies in Computational Intelligence, 2010, , 89-107.	0.7	0
166	Evolutionary Analog IC Design Optimization. Studies in Computational Intelligence, 2010, , 49-88.	0.7	0
167	FUGA. , 2009, , .		0
168	Using GAs to balance technical indicators on stock picking for financial portfolio composition. , 2009, , .		6
169	Reconfigurable multi-mode sigmaâ€“delta modulator for 4G mobile terminals. The Integration VLSI Journal, 2009, 42, 34-46.	1.3	27
170	Enhancing analog IC design optimization kernels with simple fuzzy models. , 2009, , .		2
171	Overview of radiation effects and design constraints off fully custom SMPS. , 2008, , .		5
172	A reconfigurable A/D converter for 4G wireless systems. , 2008, , .		0
173	Design of a multimode reconfigurable sigma-delta converter for 4G wireless receivers. , 2007, , .		2
174	An evolutionary optimization kernel using a dynamic GA-SVM model applied to analog IC design. , 2007, , .		5
175	Fuzzy Boolean Nets Based Paediatrics First Aid Diagnosis. , 2007, , .		4
176	Automatic analog IC layout generation based on a evolutionary computation approach. , 2007, , .		0
177	GA-SVM feasibility model and optimization kernel applied to analog IC design automation. , 2007, , .		24
178	GA-SVM Optimization Kernel applied to Analog IC Design Automation. , 2006, , .		6
179	AIDA: Analog IC Design Automation based on a Fully Configurable Design Hierarchy and Flow. , 2006, , .		0
180	Laygen - An evolutionary approach to automatic analog IC layout generation. , 2005, , .		7

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181	Enhancing the SCORM metadata model. , 2004, , .		8
182	Analogue and Mixed-Signal Systems Topologies Exploration Using Symbolic Methods. Analog Integrated Circuits and Signal Processing, 2002, 31, 161-176.	0.9	15
183	Algorithm-driven synthesis of data conversion architectures. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1997, 16, 1116-1135.	1.9	18
184	Flexible silicon compilation of charge redistribution data conversion systems. , 0, , .		3
185	RAPID-retargetability for reusability of application-driven quadrature D/A interface block design. , 0, , .		4
186	Symbolic techniques applied to switched-current ADCs synthesis. , 0, , .		0
187	A SKILL/sup TM/-based library for retargetable embedded analog cores. , 0, , .		1
188	IC design automation from circuit level optimization to retargetable layout. , 0, , .		3
189	GENOM: circuit-level optimizer based on a modified genetic algorithm kernel. , 0, , .		5
190	VIANET-a new Web framework for distance learning. , 0, , .		7
191	Enhanced genetic algorithm kernel applied to a circuit-level optimization E-design environment. , 0, , .		7
192	A multi-level model for tracking analysis in E-learning platforms. , 0, , .		0
193	Enhancing the SCORM modelling scope. , 0, , .		4
194	An evolutionary optimization kernel with adaptive parameters applied to analog circuit design. , 0, , .		9
195	Design automation methodology for analog IC design matching designers approach. , 0, , .		0
196	LAYGEN - Automatic Layout Generation of Analog ICs from Hierarchical Template Descriptions. , 0, , .		18