

Suman Lata Tripathi

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	Design of tunnel FET architectures for low power application using improved Chimp optimizer algorithm. <i>Engineering With Computers</i> , 2023, 39, 1415-1458.	6.1	10
2	A boosted chimp optimizer for numerical and engineering design optimization challenges. <i>Engineering With Computers</i> , 2023, 39, 2463-2514.	6.1	12
3	Comprehensive Analysis of 7T SRAM Cell Architectures with 18nm FinFET for Low Power Bio-Medical Applications. <i>Silicon</i> , 2022, 14, 5213-5224.	3.3	17
4	Robustness evaluation of electrical characteristics of sub-22Ånm FinFETs affected by physical variability. <i>Materials Today: Proceedings</i> , 2022, 49, 2245-2252.	1.8	6
5	18nm n-channel and p-channel Dopingless Asymmetrical Junctionless DG-MOSFET: Low Power CMOS Based Digital and Memory Applications. <i>Silicon</i> , 2022, 14, 6435-6446.	3.3	26
6	Variability Analysis of SBOX With CMOS 45Ånm Technology. <i>Wireless Personal Communications</i> , 2022, 124, 671-682.	2.7	4
7	Implementation of Low Power Inverter using Si1-xGex Pocket N & P-Channel Junction-Less Double Gate TFET. <i>Silicon</i> , 2022, 14, 9129-9142.	3.3	10
8	Effect of Mole fraction and Fin Material on Performance Parameter of 14Ånm Heterojunction Si1-xGex FinFET and Application as an Inverter. <i>Silicon</i> , 2022, 14, 8793-8804.	3.3	12
9	Impact & Analysis of Inverted-T shaped Fin on the Performance parameters of 14-nm heterojunction FinFET. <i>Silicon</i> , 2022, 14, 9441-9451.	3.3	2
10	Augmenting Mental Healthcare With Artificial Intelligence, Machine Learning, and Challenges in Telemedicine. <i>Advances in Computational Intelligence and Robotics Book Series</i> , 2022, , 75-90.	0.4	4
11	Analytical Model of Dopingless Asymmetrical Junctionless Double Gate MOSFET. <i>Silicon</i> , 2022, 14, 10765-10774.	3.3	3
12	Improved Drain Current with Suppressed Short Channel Effect of P-Pocket Double-Gate MOSFET in Sub-14Ånm Technology Node. <i>Silicon</i> , 2022, 14, 10881-10891.	3.3	5
13	Coronavirus. , 2022, , 109-117.		1
14	Machine Learning Classifiers for Speech Detection. , 2022, , .		7
15	An Efficient Approach to Design a Comparator for SAR-ADC. , 2022, , .		2
16	Leakage Reduction in 18Ånm FinFET based 7T SRAM Cell using Self Controllable Voltage Level Technique. <i>Wireless Personal Communications</i> , 2021, 116, 1837-1847.	2.7	19
17	DG MOSFET for Bio-Sensing Applications: A Review. , 2021, , .		3
18	Double Gate-Pocket-Junction-less Tunnel Field Effect Transistor. , 2021, , .		1

#	ARTICLE	IF	CITATIONS
19	Power Dissipation Estimation in SWCNT based Interconnects. , 2021, , .		0
20	A Novel Junction Less Dual Gate Tunnel FET with SiGe Pocket for Low Power Applications. , 2021, , .		5
21	Impact of Channel Engineering on 16nm, 18nm & 20nm Doping-less DG MOSFET. , 2021, , .		3
22	Process evaluation in FinFET based 7T SRAM cell. Analog Integrated Circuits and Signal Processing, 2021, 109, 545-551.	1.4	14
23	Accurate Detection and Diagnosis of Breast Cancer Using Scaled Conjugate Gradient Back Propagation Algorithm and Advanced Deep Learning Techniques. Lecture Notes in Electrical Engineering, 2021, , 99-112.	0.4	3
24	Column shifting algorithm to compute iteration bound of finite impulse response systems having inline delays. International Journal of Embedded Systems, 2021, 14, 443.	0.3	0
25	Enhanced Performance Double-gate Junction-less Tunnel Field Effect Transistor for Bio-Sensing Application. Solid State Electronics Letters, 2021, 3, 19-26.	1.0	3
26	Low Power Efficient Si _{0.7} Ge _{0.3} Pocket Junction-Less DGTfET with Sensing Ability for Bio-species. Algorithms for Intelligent Systems, 2020, , 1395-1403.	0.6	0
27	Design of Low Power Si _{0.7} Ge _{0.3} Pocket Junction-Less Tunnel FET Using Below 5Ånm Technology. Wireless Personal Communications, 2020, 111, 2167-2176.	2.7	17
28	(Ba/Pb) _x Sr _{1-x} TiO ₃ based capacitive sensor with LaNiO ₃ electrode for higher tunability. Journal of Materials Science: Materials in Electronics, 2020, 31, 20387-20399.	2.2	2
29	SBOX under PVT variation. Analog Integrated Circuits and Signal Processing, 2020, 105, 73-82.	1.4	2
30	Comparative Analysis of Leakage Power in 18nm 7T and 8T SRAM cell Implemented with SVL Technique. , 2020, , .		9
31	Analysis of gate engineered asymmetric junctionless double gate MOSFET for varying operating conditions. IOP Conference Series: Materials Science and Engineering, 2020, 872, 012012.	0.6	1
32	Design of Low Power 7T SRAM Cell for portable Biomedical Applications. , 2020, , .		5
33	A review on performance comparison of advanced MOSFET structures below 45 nm technology node. Journal of Semiconductors, 2020, 41, 061401.	3.7	46
34	A Journey from Bulk MOSFET to 3Ånm and Beyond. Transactions on Electrical and Electronic Materials, 2020, 21, 443-455.	1.9	26
35	Low-Power Efficient p+ Si _{0.7} Ge _{0.3} Pocket Junctionless SGTfET with Varying Operating Conditions. Journal of Electronic Materials, 2020, 49, 4291-4299.	2.2	20
36	Design and Analysis of Heavily Doped n+ Pocket Asymmetrical Junction-Less Double Gate MOSFET for Biomedical Applications. Applied Sciences (Switzerland), 2020, 10, 2499.	2.5	27

#	ARTICLE	IF	CITATIONS
37	Low-Power High-Performance Tunnel FET With Analysis for IoT Applications. Advances in Computational Intelligence and Robotics Book Series, 2020, , 47-67.	0.4	3
38	Strategic Review on Different Materials for FinFET Structure Performance Optimization. IOP Conference Series: Materials Science and Engineering, 2020, 988, 012054.	0.6	6
39	Static Timing Analysis of Sequential Circuit with GUI. , 2020, , .		1
40	Design for Testability of High-Speed Advance Multipliers. Advances in Computational Intelligence and Robotics Book Series, 2020, , 175-190.	0.4	0
41	Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications. , 2019, , .		19
42	Low leakage pocket junction-less DGTFET with biosensing cavity region. Turkish Journal of Electrical Engineering and Computer Sciences, 2019, 27, 2466-2474.	1.4	17
43	Characterisation of Ultra-Small Pocket Si _{0.7} Ge _{0.3} Junction-less Tunnel FET with SOI. , 2019, , .		2
44	Asymmetric gated Ge-Si$\geq 0.7\text{Ge}$0.3 nHTFET and pHTFET for steep subthreshold characteristics. International Journal of Microstructure and Materials Properties, 2019, 14, 497.	0.1	5
45	A Novel Design of All Digital Phase Locked Loop for Wireless Applications. , 2019, , .		1
46	Performance Analysis of Double Gate Heterojunction Tunnel Field Effect Transistor. , 2019, , .		4
47	Subthreshold Performance Evaluation of JLDG-MOSFET. , 2019, , .		3
48	Analysis and Design of high-K Material Nanowire Transistor for Improved Performance. , 2019, , .		4
49	Asymmetric Gated Ge-Si _{0.7} Ge _{0.3} nHTFET and pHTFET for Steep Subthreshold Characteristics. International Journal of Microstructure and Materials Properties, 2019, 14, 1.	0.1	1
50	Mole-Fraction Engineering in Germanium Source Pocket Based Tunnel Field Effect Transistor. Sensor Letters, 2019, 17, 470-473.	0.4	0
51	Pocket Vertical Junction-Less U-Shape Tunnel FET and Its Challenges in Nano-Scale Regime. Advanced Science, Engineering and Medicine, 2019, 11, 1225-1230.	0.3	0
52	High Performance Low Leakage Pocket Si _x Ge _{1-x} Junction-Less Single-Gate Tunnel FET for 10 nm Technology. , 2018, , .		4
53	Analysis of Different Characteristics of SOI-TFET with Ge Material as Source Pocket. , 2018, , .		1
54	Performance Enhanced Unsymmetrical FinFET and its Applications. , 2018, , .		6

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55	Design of Triple Material Junctionless CG MOSFET. , 2018, , .		6
56	Speed Enhancement in the Performance of Two Phase Clocked Adiabatic Static CMOS Logic Circuits. , 2018, , .		1
57	BDD Based Logic Synthesis and Optimization for Low Power Comparator Circuit. , 2018, , .		1
58	The Effects of Variation in Geometry Parameters on Sub-50 nm Finfet and Their Direct Impact on Finfet Performance. , 2018, , .		0
59	METAPUF: A challenge response pair generator. Periodicals of Engineering and Natural Sciences, 2018, 6, 58.	0.5	2
60	Low power design of bulk driven operational transconductance amplifier. , 2017, , .		9
61	Triple-band microstrip patch antenna with improved gain. , 2016, , .		5
62	High performance Bulk FinFET with bottom spacer. , 2013, , .		7
63	Characteristic comparison of connected DG FINFET, TG FINFET and Independent Gate FINFET on 32 nm technology. , 2012, , .		16
64	Process variation and analysis of FinFET for low-power applications. IOP Conference Series: Materials Science and Engineering, 0, 872, 012015.	0.6	6
65	Electrical Characterization of highly stable 10nm triple-gate FinFET for different contacts and oxide region materials. Silicon, 0, , 1.	3.3	5