Suman Lata Tripathi

List of Publications by Year
in descending order

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65	473	933447	940533
papers	citations	10 h-index	16 g-index

72	72	72	87
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A review on performance comparison of advanced MOSFET structures below 45 nm technology node. Journal of Semiconductors, 2020, 41, 061401.	3.7	46
2	Design and Analysis of Heavily Doped n+ Pocket Asymmetrical Junction-Less Double Gate MOSFET for Biomedical Applications. Applied Sciences (Switzerland), 2020, 10, 2499.	2.5	27
3	A Journey from Bulk MOSFET to 3Ânm and Beyond. Transactions on Electrical and Electronic Materials, 2020, 21, 443-455.	1.9	26
4	18nm n-channel and p-channel Dopingless Asymmetrical Junctionless DG-MOSFET: Low Power CMOS Based Digital and Memory Applications. Silicon, 2022, 14, 6435-6446.	3.3	26
5	Low-Power Efficient p+ Si0.7Ge0.3 Pocket Junctionless SGTFET with Varying Operating Conditions. Journal of Electronic Materials, 2020, 49, 4291-4299.	2.2	20
6	Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications. , 2019, , .		19
7	Leakage Reduction in 18Ânm FinFET based 7T SRAM Cell using Self Controllable Voltage Level Technique. Wireless Personal Communications, 2021, 116, 1837-1847.	2.7	19
8	Low leakage pocket junction-less DGTFET with biosensing cavity region. Turkish Journal of Electrical Engineering and Computer Sciences, 2019, 27, 2466-2474.	1.4	17
9	Design of Low Power Si0.7Ge0.3 Pocket Junction-Less Tunnel FET Using Below 5Ânm Technology. Wireless Personal Communications, 2020, 111, 2167-2176.	2.7	17
10	Comprehensive Analysis of 7T SRAM Cell Architectures with 18nm FinFET for Low Power Bio-Medical Applications. Silicon, 2022, 14, 5213-5224.	3.3	17
11	Characteristic comparison of connected DG FINFET, TG FINFET and Independent Gate FINFET on 32 nm technology. , 2012, , .		16
12	Process evaluation in FinFET based 7T SRAM cell. Analog Integrated Circuits and Signal Processing, 2021, 109, 545-551.	1.4	14
13	Effect of Mole fraction and Fin Material on Performance Parameter of 14Ânm Heterojunction Si1-xGex FinFET and Application as an Inverter. Silicon, 2022, 14, 8793-8804.	3.3	12
14	A boosted chimp optimizer for numerical and engineering design optimization challenges. Engineering With Computers, 2023, 39, 2463-2514.	6.1	12
15	Design of tunnel FET architectures for low power application using improved Chimp optimizer algorithm. Engineering With Computers, 2023, 39, 1415-1458.	6.1	10
16	Implementation of Low Power Inverter using Si1-xGex Pocket N & P-Channel Junction-Less Double Gate TFET. Silicon, 2022, 14, 9129-9142.	3.3	10
17	Low power design of bulk driven operational transconductance amplifier. , 2017, , .		9
18	Comparative Analysis of Leakage Power in 18nm 7T and 8T SRAM cell Implemented with SVL Technique. , 2020, , .		9

#	Article	IF	Citations
19	High performance Bulk FinFET with bottom spacer. , 2013, , .		7
20	Machine Learning Classifiers for Speech Detection. , 2022, , .		7
21	Performance Enhanced Unsymmetrical FinFET and its Applications. , 2018, , .		6
22	Design of Triple Material Junctionless CG MOSFET. , 2018, , .		6
23	Process variation and analysis of FinFET for low-power applications. IOP Conference Series: Materials Science and Engineering, 0, 872, 012015.	0.6	6
24	Robustness evaluation of electrical characteristics of sub-22Ânm FinFETs affected by physical variability. Materials Today: Proceedings, 2022, 49, 2245-2252.	1.8	6
25	Strategic Review on Different Materials for FinFET Structure Performance Optimization. IOP Conference Series: Materials Science and Engineering, 2020, 988, 012054.	0.6	6
26	Triple-band microstrip patch antenna with improved gain. , 2016, , .		5
27	Asymmetric gated Ge-Si<SUB align="right">0.7Ge<SUB align="right">0.3 nHTFET and pHTFET for steep subthreshold characteristics. International Journal of Microstructure and Materials Properties, 2019, 14, 497.	0.1	5
28	Design of Low Power 7T SRAM Cell for portable Biomedical Applications. , 2020, , .		5
29	A Novel Junction Less Dual Gate Tunnel FET with SiGe Pocket for Low Power Applications. , 2021, , .		5
30	Improved Drain Current with Suppressed Short Channel Effect of pâ€‰+â€‰Pocket Double-Gate MOSFET in Sub-14Ânm Technology Node. Silicon, 2022, 14, 10881-10891.	3.3	5
31	Electrical Characterization of highly stable 10nm triple-gate FinFET for different contacts and oxide region materials. Silicon, 0, , 1.	3.3	5
32	High Performance Low Leakage Pocket Si_xGe_{1-x} Junction-Less Single-Gate Tunnel FET for 10 nm Technology. , 2018, , .		4
33	Performance Analysis of Double Gate Heterojunction Tunnel Field Effect Transistor. , 2019, , .		4
34	Analysis and Design of high-K Material Nanowire Transistor for Improved Performance. , 2019, , .		4
35	Variability Analysis of SBOX With CMOS 45Ânm Technology. Wireless Personal Communications, 2022, 124, 671-682.	2.7	4
36	Augmenting Mental Healthcare With Artificial Intelligence, Machine Learning, and Challenges in Telemedicine. Advances in Computational Intelligence and Robotics Book Series, 2022, , 75-90.	0.4	4

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37	Subthreshold Performance Evaluation of JLDG-MOSFET. , 2019, , .		3
38	DG MOSFET for Bio-Sensing Applications: A Review. , 2021, , .		3
39	Impact of Channel Engineering on 16nm, 18nm & 20nm Doping-less DG MOSFET. , 2021, , .		3
40	Accurate Detection and Diagnosis of Breast Cancer Using Scaled Conjugate Gradient Back Propagation Algorithm and Advanced Deep Learning Techniques. Lecture Notes in Electrical Engineering, 2021, , 99-112.	0.4	3
41	Low-Power High-Performance Tunnel FET With Analysis for IoT Applications. Advances in Computational Intelligence and Robotics Book Series, 2020, , 47-67.	0.4	3
42	Analytical Model of Dopingless Asymmetrical Junctionless Double Gate MOSFET. Silicon, 2022, 14, 10765-10774.	3.3	3
43	Enhanced Performance Double-gate Junction-less Tunnel Field Effect Transistor for Bio-Sensing Application. Solid State Electronics Letters, 2021, 3, 19-26.	1.0	3
44	Characterisation of Ultra-Small Pocket Si_{0.7}Ge_{0.3} Junction-less Tunnel FET with SOI. , 2019, , .		2
45	(Ba/Pb)xSr1âˆ'xTiO3 based capacitive sensor with LaNiO3 electrode for higher tunability. Journal of Materials Science: Materials in Electronics, 2020, 31, 20387-20399.	2.2	2
46	SBOX under PVT variation. Analog Integrated Circuits and Signal Processing, 2020, 105, 73-82.	1.4	2
47	METAPUF: A challenge response pair generator. Periodicals of Engineering and Natural Sciences, 2018, 6, 58.	0.5	2
48	Impact & Analysis of Inverted-T shaped Fin on the Performance parameters of 14-nm heterojunction FinFET. Silicon, 2022, 14, 9441-9451.	3.3	2
49	An Efficient Approach to Design a Comparator for SAR-ADC. , 2022, , .		2
50	Analysis of Different Characteristics of SOI-TFET with Ge Material as Source Pocket. , 2018, , .		1
51	Speed Enhancement in the Performance of Two Phase Clocked Adiabatic Static CMOS Logic Circuits. , 2018, , .		1
52	BDD Based Logic Synthesis and Optimization for Low Power Comparator Circuit. , 2018, , .		1
53	A Novel Design of All Digital Phase Locked Loop for Wireless Applications. , 2019, , .		1
54	Analysis of gate engineered asymmetric junctionless double gate MOSFET for varying operating conditions. IOP Conference Series: Materials Science and Engineering, 2020, 872, 012012.	0.6	1

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55	Double Gate-Pocket-Junction-less Tunnel Field Effect Transistor. , 2021, , .		1
56	Asymmetric Gated Ge-Si0.7Ge0.3 nHTFET and pHTFET for Steep Subthreshold Characteristics. International Journal of Microstructure and Materials Properties, 2019, 14, 1.	0.1	1
57	Static Timing Analysis of Sequential Circuit with GUI. , 2020, , .		1
58	Coronavirus. , 2022, , 109-117.		1
59	The Effects of Variation in Geometry Parameters on Sub-50 nm Finfet and Their Direct Impact on Finfet Performance. , 2018, , .		0
60	Low Power Efficient Si0.7Ge0.3 Pocket Junction-Less DGTFET with Sensing Ability for Bio-species. Algorithms for Intelligent Systems, 2020, , 1395-1403.	0.6	0
61	Power Dissipation Estimation in SWCNT based Interconnects. , 2021, , .		0
62	Mole-Fraction Engineering in Germanium Source Pocket Based Tunnel Field Effect Transistor. Sensor Letters, 2019, 17, 470-473.	0.4	0
63	Pocket Vertical Junction-Less U-Shape Tunnel FET and Its Challenges in Nano-Scale Regime. Advanced Science, Engineering and Medicine, 2019, 11, 1225-1230.	0.3	0
64	Design for Testability of High-Speed Advance Multipliers. Advances in Computational Intelligence and Robotics Book Series, 2020, , 175-190.	0.4	0
65	Column shifting algorithm to compute iteration bound of finite impulse response systems having inline delays. International Journal of Embedded Systems, 2021, 14, 443.	0.3	0