Tohru Ishihara

List of Publications by Year
in descending order

78	976	1684188 5	1372567 10
papers	citations	h-index	g-index

79	79	79	415
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Voltage scheduling problem for dynamically variable voltage processors. , 1998, , .		615
2	Wide-Supply-Range All-Digital Leakage Variation Sensor for On-Chip Process and Temperature Monitoring. IEEE Journal of Solid-State Circuits, 2015, 50, 2475-2490.	5.4	41
3	A power reduction technique with object code merging for application specific embedded processors. , 2000, , .		20
4	An RTOS in hardware for energy efficient software-based TCP/IP processing. , 2010, , .		19
5	SRAM Leakage Reduction by Row/Column Redundancy Under Random Within-Die Delay Variation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1660-1671.	3.1	18
6	A non-uniform cache architecture for low power system design. , 2005, , .		17
7	Minimum energy point tracking using combined dynamic voltage scaling and adaptive body biasing. , 2016, , .		16
8	AMPLE: An Adaptive Multi-Performance Processor for Low-Energy Embedded Applications. , 2008, , .		13
9	Minimizing inter-task interferences in scratch-pad memory usage for reducing the energy consumption of multi-task systems. , 2010, , .		12
10	Code and Data Placement for Embedded Processors with Scratchpad and Cache Memories. Journal of Signal Processing Systems, 2010, 60, 211-224.	2.1	11
11	A built-in self-adjustment scheme with adaptive body bias using P/N-sensitive digital monitor circuits. , 2012, , .		11
12	Analysis and comparison of XOR cell structures for low voltage circuit design. , 2013, , .		11
13	Microarchitectural-level statistical timing models for near-threshold circuit design. , 2015, , .		11
14	Reconfigurable delay cell for area-efficient implementation of on-chip MOSFET monitor schemes. , 2013, , .		10
15	Task Scheduling for Reliable Cache Architectures of Multiprocessor Systems. , 2007, , .		9
16	An integrated optical parallel adder as a first step towards light speed data processing. , 2016, , .		8
17	An energy-efficient on-chip memory structure for variability-aware near-threshold operation. , 2015, , .		7
18	Fully digital on-chip memory using minimum height standard cells for near-threshold voltage computing. , 2016, , .		7

#	Article	IF	Citations
19	Code Placement for Reducing the Energy Consumption of Embedded Processors with Scratchpad and Cache Memories. , 2007, , .		6
20	Guidelines for effective and simplified dynamic supply and threshold voltage scaling. , 2016, , .		6
21	A Multi-Performance Processor for Reducing the Energy Consumption of Real-Time Embedded Systems. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 2533-2541.	0.3	6
22	A Generalized Framework for System-Wide Energy Savings in Hard Real-Time Embedded Systems. , 2008, , .		5
23	An integrated optimization framework for reducing the energy consumption of embedded real-time applications. , 2011, , .		5
24	Area-efficient fully digital memory using minimum height standard cells for near-threshold voltage computing. The Integration VLSI Journal, 2019, 65, 201-210.	2.1	5
25	An Energy Characterization Framework for Software-Based Embedded Systems. , 2006, , .		4
26	A Software Technique to Improve Yield of Processor Chips in Presence of Ultra-Leaky SRAM Cells Caused by Process Variation. , 2007, , .		4
27	Row/column redundancy to reduce SRAM leakage in presence of random within-die delay variation. , 2008, , .		4
28	Simultaneous optimization of memory configuration and code allocation for low power embedded systems. , 2008, , .		4
29	Energy reduction by built-in body biasing with single supply voltage operation. , 2015, , .		4
30	Energy Management Techniques for SOC Design. , 2006, , 177-223.		3
31	Cache Power Reduction in Presence of Within-Die Delay Variation Using Spare Ways. , 2008, , .		3
32	A flexible structure of standard cell and its optimization method for near-threshold voltage operation. , 2012, , .		3
33	A Standard Cell Optimization Method for Near-Threshold Voltage Operations. Lecture Notes in Computer Science, 2013, , 32-41.	1.3	3
34	Wide-supply-range all-digital leakage variation sensor for on-chip process and temperature monitoring. , 2014, , .		3
35	Analytical Stability Modeling for CMOS Latches in Low Voltage Operation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2016, E99.A, 2463-2472.	0.3	3
36	A closed-form stability model for cross-coupled inverters operating in sub-threshold voltage region. , 2016, , .		3

#	Article	IF	Citations
37	Minimum Energy Point Tracking with All-Digital On-Chip Sensors. Journal of Low Power Electronics, 2018, 14, 227-235.	0.6	3
38	Statistical Timing Modeling Based on a Lognormal Distribution Model for Near-Threshold Circuit Optimization. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2015, E98.A, 1455-1466.	0.3	3
39	An Integrated Framework for Energy Optimization of Embedded Real-Time Applications. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 2477-2487.	0.3	3
40	A Necessary and Sufficient Condition of Supply and Threshold Voltages in CMOS Circuits for Minimum Energy Point Operation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 2764-2775.	0.3	3
41	Flexible System LSI for Embedded Systems and Its Optimization Techniques. Design Automation for Embedded Systems, 2000, 5, 179-205.	1.0	2
42	Processor Energy Characterization for Compiler-Assisted Software Energy Reduction. Journal of Electrical and Computer Engineering, 2012, 2012, 1-16.	0.9	2
43	I/O aware task scheduling for energy harvesting embedded systems with PV and capacitor arrays. , 2012, , .		2
44	Variation-aware Flip-Flop energy optimization for ultra low voltage operation. , 2014, , .		2
45	Design methodology of process variation tolerant D-Flip-Flops for low voltage circuit operation. , 2014, , .		2
46	Layout Generator with Flexible Grid Assignment for Area Efficient Standard Cell. IPSJ Transactions on System LSI Design Methodology, 2015, 8, 131-135.	0.8	2
47	On-chip temperature and process variation sensing using a reconfigurable Ring Oscillator. , 2017, , .		2
48	Real-Time Minimum Energy Point Tracking Using a Predetermined Optimal Voltage Setting Strategy. , 2020, , .		2
49	DC-DC Converter-Aware Task Scheduling and Dynamic Reconfiguration for Energy Harvesting Embedded Systems. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 2660-2667.	0.3	2
50	Analysis of Effects of Input Arrival Time Variations on On-Chip Bus Power Consumption. Lecture Notes in Computer Science, 2009, , 62-71.	1.3	2
51	Implementation of Stack Data Placement and Run Time Management Using a Scratch-Pad Memory for Energy Consumption Reduction of Embedded Applications. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 2597-2608.	0.3	2
52	A single cycle accessible two-level cache architecture for reducing the energy consumption of embedded systems. , 2008, , .		1
53	Redundancy techniques for SRAM leakage reduction in presence of within-die delay variation. , 2008, , .		1
54	Real-Time power management for a multi-performance processor. , 2009, , .		1

#	Article	IF	Citations
55	Optimal stack frame placement and transfer for energy reduction targeting embedded processors with scratch-pad memories. , 2009, , .		1
56	DLIC. Transactions on Embedded Computing Systems, 2013, 13, 1-26.	2.9	1
57	Variability- and correlation-aware logical effort for near-threshold circuit design. , 2016, , .		1
58	A Minimum Energy Point Tracking Algorithm Based on Dynamic Voltage Scaling and Adaptive Body Biasing. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 2776-2784.	0.3	1
59	Maximizing Energy Efficiency of on-Chip Caches Exploiting Hybrid Memory Structure. , 2018, , .		1
60	Integration of Minimum Energy Point Tracking and Soft Real-Time Scheduling for Edge Computing. , 2021, , .		1
61	Unified Gated Flip-Flops for Reducing the Clocking Power in Register Circuits. Lecture Notes in Computer Science, 2011, , 237-246.	1.3	1
62	Standard Cell Structure with Flexible P/N Well Boundaries for Near-Threshold Voltage Operation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 2499-2507.	0.3	1
63	Variation-Aware Software Techniques for Cache Leakage Reduction Using Value-Dependence of SRAM Leakage Due to Within-Die Process Variation. , 2008, , 224-239.		1
64	A software technique to improve lifetime of caches containing ultra-leaky SRAM cells caused by within-die Vth variation. Microelectronics Journal, 2008, 39, 1797-1808.	2.0	0
65	A generalized framework for energy savings in real-time multiprocessor systems. , 2008, , .		0
66	Instruction cache leakage reduction by changing register operands and using asymmetric sram cells. , 2008, , .		0
67	Value-dependence of SRAM leakage in deca-nanometer technologies. IEICE Electronics Express, 2008, 5, 23-28.	0.8	0
68	Single-Cycle-Accessible Two-Level Caches and Compilation Technique for Energy Reducion. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 189-199.	0.8	0
69	An Optimization Technique for Low-Energy Embedded Memory Systems. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 239-249.	0.8	0
70	An implementation of energy efficient multi-performance processor for real-time applications. , 2010, , .		0
71	Loop instruction caching for energy-efficient embedded multitasking processors. , 2012, , .		0
72	An impact of process variation on supply voltage dependence of logic path delay variation. , 2015, , .		0

#	Article	IF	Citations
73	A temperature monitor circuit with small voltage sensitivity using a topology-reconfigurable ring oscillator. Japanese Journal of Applied Physics, 2018, 57, 04FF09.	1.5	0
74	Approximate Minimum Energy Point Tracking and Task Scheduling for Energy-Efficient Real-Time Computing. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2022, E105.A, 518-529.	0.3	0
75	Low-Power Design Methodology of Voltage Over-Scalable Circuit with Critical Path Isolation and Bit-Width Scaling. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2021, , .	0.3	0
76	Software-Level Instruction-Cache Leakage Reduction Using Value-Dependence of SRAM Leakage in Nanometer Technologies. Lecture Notes in Computer Science, 2011, , 275-299.	1.3	0
77	A Design Method of a Cell-Based Amplifier for Body Bias Generation. IEICE Transactions on Electronics, 2019, E102.C, 565-572.	0.6	0
78	Energy-Efficient Embedded System Design at 90nm and Below â€“ A System-Level Perspective â€“. , 2005, , 452-465.		0