Naushad Alam

List of Publications by Year
in descending order

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57	625	840585	642610
papers	citations	11	23
		h-index	g-index

58	58	58	318
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2634-2642.	2.1	128
2	Low Leakage Single Bitline 9 T (SB9T) Static Random Access Memory. Microelectronics Journal, 2017, 62, 1-11.	1.1	55
3	Low Leakage Fully Half-Select-Free Robust SRAM Cells With BTI Reliability Analysis. IEEE Transactions on Device and Materials Reliability, 2018, 18, 337-349.	1.5	54
4	Robust TFET SRAM cell for ultra-low power IoT applications. AEU - International Journal of Electronics and Communications, 2018, 89, 70-76.	1.7	49
5	Pseudo differential multi-cell upset immune robust SRAM cell for ultra-low power applications. AEU - International Journal of Electronics and Communications, 2018, 83, 366-375.	1.7	48
6	Dopingless Tunnel Field-Effect Transistor With Oversized Back Gate: Proposal and Investigation. IEEE Transactions on Electron Devices, 2018, 65, 4701-4708.	1.6	37
7	TFET-Based Robust 7T SRAM Cell for Low Power Application. IEEE Transactions on Electron Devices, 2019, 66, 3834-3840.	1.6	32
8	Impact of asymmetric dual-k spacers on tunnel field effect transistors. Journal of Computational Electronics, 2018, 17, 756-765.	1.3	20
9	Multifinger MOSFETsâ€™ Optimization Considering Stress and INWE in Static CMOS Circuits. IEEE Transactions on Electron Devices, 2016, 63, 2517-2523.	1.6	14
10	Performance Enhancement of Junctionless Tunnel Field Effect Transistor Using Dual-k Spacers. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 912-920.	0.1	14
11	Effective Current Model for Inverter-Transmission Gate Structure and Its Application in Circuit Design. IEEE Transactions on Electron Devices, 2017, 64, 4002-4010.	1.6	13
12	Systematic design of CNTFET based OTA and Op amp using gm/ID technique. Analog Integrated Circuits and Signal Processing, 2020, 102, 293-307.	0.9	11
13	Efficient ECSM Characterization Considering Voltage, Temperature, and Mechanical Stress Variability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 3407-3415.	3.5	10
14	Suppression of ambipolarity in tunnelâ€FETs using gate oxide as parameter: analysis and investigation. IET Circuits, Devices and Systems, 2020, 14, 288-293.	0.9	9
15	Gate-Pitch Optimization for Circuit Design Using Strain-Engineered Multifinger Gate Structures. IEEE Transactions on Electron Devices, 2012, 59, 3120-3123.	1.6	8
16	Process induced mechanical stress aware poly-pitch optimization for enhanced circuit performance. , 2012, , .		8
17	CNTFET Based Circuit Design for Improved Performance. , 2019, , .		7
18	Design of a triple pocket multi-gate material TFET structure for low-power applications. Semiconductor Science and Technology, 2021, 36, 025015.	1.0	7

#	Article	IF	Citations
19	Carbon nanotube interconnects for low-power high-speed applications. , 2009, , .		6
20	An Analytical Delay Model for Mechanical Stress Induced Systematic Variability Analysis in Nanoscale Circuit Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1714-1726.	3.5	6
21	Effective Drive Current for Near-Threshold CMOS Circuitsâ€™ Performance Evaluation: Modeling to Circuit Design Techniques. IEEE Transactions on Electron Devices, 2018, 65, 2413-2421.	1.6	6
22	Electrostatically doped drain junctionless transistor for low-power applications. Journal of Computational Electronics, 2019, 18, 864-871.	1.3	6
23	Design of CNTFET-Based CCII Using gm/ID Technique for Low-Voltage and Low-Power Applications. Journal of Circuits, Systems and Computers, 2020, 29, 2050143.	1.0	6
24	A variation aware timing model for a 2-input NAND gate and its use in sub-65 nm CMOS standard cell characterization. Microelectronics Journal, 2016, 53, 45-55.	1.1	5
25	Performance Improvement of Tunnel Field Effect Transistor Using Double Pocket. Journal of Nanoelectronics and Optoelectronics, 2019, 14, 1148-1157.	0.1	5
26	A Robust 10T SRAM Cell with Enhanced Read Operation. International Journal of Computer Applications, 2015, 129, 7-12.	0.2	5
27	Comparison of Parallel Prefix Adders Based on FPGA & ASIC Implementations. , 2020, , .		5
28	Analysis of carbon nanotube interconnects and their comparison with Cu interconnects. , 2009, , .		4
29	The impact of process-induced mechanical stress on CMOS buffer design using multi-fingered devices. Microelectronics Reliability, 2013, 53, 379-385.	0.9	4
30	FPGA and ASIC Implementation and Comparison of Multipliers. , 2020, , .		4
31	Performance Improvement of Dopingless Transistor for Low Power Applications. Silicon, 2022, 14, 8009-8020.	1.8	4
32	Performance comparison and variability analysis of CNT bundle and Cu interconnects. , 2009, , .		3
33	An analytical delay model for CMOS Inverter-Transmission Gate structure. , 2014, , .		3
34	Soft error hardened symmetric SRAM cell with high read stability. , 2017, , .		3
35	Design of TFET based Op-Amp and CCII for low voltage and low power applications. International Journal of Electronics, 2021, 108, 1733-1753.	0.9	3
36	Subthreshold deep submicron performance investigation of CMOS and DTCMOS biasing schemes for reconfigurable computing. , 2009, , .		2

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37	The impact of process-induced mechanical stress in narrow width devices and variable-taper CMOS buffer design. Microelectronics Reliability, 2013, 53, 718-724.	0.9	2
38	Pre-layout estimation of performance and design of basic analog circuits in stress enabled technologies. , 2015, , .		2
39	Robust TFET SRAM cell for ultra-low power IoT application. , 2017, , .		2
40	Compact and Reliable Low Power Non-Volatile TCAM Cell. , 2018, , .		2
41	Modeling the effect of variability on the timing response of CMOS inverter-transmission gate structure. , 2018, , .		2
42	Pocket engineered electrostatically doped tunnel field effect transistor. , 2019, , .		2
43	Design approach to improve the performance of JAMFETs. IET Circuits, Devices and Systems, 2020, 14, 333-339.	0.9	2
44	Radiation Hardened Area-Efficient 10T SRAM Cell for Space Applications. , 2021, , .		2
45	A 9 T SRAM cell with data-independent read bitline leakage and improved read sensing margin for low power applications. Semiconductor Science and Technology, 2022, 37, 055001.	1.0	2
46	The Impact of Process-Induced Mechanical Stress in Narrow Width Devices and Circuit Design Issues. , 2012, , .		1
47	Low leakage write-enhanced robust 11T SRAM cell with fully half-select-free operation. , 2017, , .		1
48	Analysis of Pocket Tunnel Field Effect Transistor. , 2020, , .		1
49	The impact of process-induced mechanical stress on multi-fingered device performance. Proceedings of SPIE, 2012, , .	0.8	0
50	The impact of process-induced mechanical stress on d-latch timing performance. , 2013, , .		0
51	Robust TFET SRAM cell for ultra-low power IoT application. , 2017, , .		0
52	Investigation of BTI effects on sense amplifiers. , 2017, , .		0
53	UTBB FD-SOI Circuit Design using Multifinger Transistors: A Circuit-Device Interaction Perspective. , 2018, , .		0
54	Compact and Low Power 11T-2MTJ Non-Volatile Ternary Content Addressable Memory Cell with High Sense Margin. Journal of Low Power Electronics, 2019, 15, 193-203.	0.6	0

#	Article	IF	Citations
55	Low-Power Memory Design for IoT-Enabled Systems. , 2021, , 43-62.		0
56	CNTFET based radiation hardened latch. Australian Journal of Electrical and Electronics Engineering, 2021, 18, 199-208.	0.7	0
57	Impact of Pocket-Size Variation on the Performance of GaAs_{0.1}Sb_{0.9}/InAs Based Heterojunction Double Gate Tunnel Field Effect Transistor. Journal of Nanoelectronics and Optoelectronics, 2018, 13, 1009-1018.	0.1	0