Dimitris Gizopoulos

List of Publications by Year
in descending order

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120	2,160	430442	395343
papers	citations	18	33
		h-index	g-index

122	122	122	638
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	On the Evaluation of the Total-Cost-of-Ownership Trade-Offs in Edge vs Cloud Deployments: A Wireless-Denial-of-Service Case Study. IEEE Transactions on Sustainable Computing, 2022, 7, 334-345.	2.2	5
2	The Impact of CPU Voltage Margins on Power-Constrained Execution. IEEE Transactions on Sustainable Computing, 2022, 7, 221-234.	2.2	11
3	gpuFI-4: A Microarchitecture-Level Framework for Assessing the Cross-Layer Resilience of Nvidia GPUs. , 2022, , .		4
4	Robust System Design IEEE IOLTS 2021. IEEE Transactions on Device and Materials Reliability, 2022, 22, 95-97.	1.5	0
5	The Impact of SoC Integration and OS Deployment on the Reliability of Arm Processors. , 2021, , .		5
6	Demystifying the System Vulnerability Stack: Transient Fault Effects Across the Layers. , 2021, , .		24
7	Boosting Microprocessor Efficiency: Circuit- and Workload-Aware Assessment of Timing Errors. , 2021, , .		6
8	Characterizing Soft Error Vulnerability of CPUs Across Compiler Optimizations and Microarchitectures. , 2021, , .		8
9	Editorialâ€"Robust System Design IEEE IOLTS 2019. IEEE Transactions on Device and Materials Reliability, 2020, 20, 293-294.	1.5	0
10	Cross-Layer Soft-Error Resilience Analysis of Computing Systems. , 2020, , .		0
11	rACE: Reverse-Order Processor Reliability Analysis. , 2020, , .		1
12	Exceeding Conservative Limits: A Consolidated Analysis on Modern Hardware Margins. IEEE Transactions on Device and Materials Reliability, 2020, 20, 341-350.	1.5	21
13	Demystifying Soft Error Assessment Strategies on ARM CPUs: Microarchitectural Fault Injection vs. Neutron Beam Experiments. , 2019, , .		34
14	Assessing the Effects of Low Voltage in Branch Prediction Units. , 2019, , .		13
15	Guest Editorial Robust System Design: IEEE International On-Line Testing and Robust System Design Symposium (IOLTS) 2018. IEEE Transactions on Device and Materials Reliability, 2019, 19, 3-5.	1.5	0
16	Adaptive Voltage/Frequency Scaling and Core Allocation for Balanced Energy and Performance on Multicore CPUs. , 2019, , .		27
17	Multi-Bit Upsets Vulnerability Analysis of Modern Microprocessors. , 2019, , .		16
18	Improving the Energy Efficiency by Exceeding the Conservative Operating Limits. , 2019, , 241-271.		0

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19	SyRA: Early System Reliability Analysis for Cross-Layer Soft Errors Resilience in Memory Arrays of Microprocessor Systems. IEEE Transactions on Computers, 2019, 68, 765-783.	2.4	27
20	HealthLog Monitor: Errors, Symptoms and Reactions Consolidated. IEEE Transactions on Device and Materials Reliability, 2019, 19, 46-54.	1.5	5
21	Statistical Analysis of Multicore CPUs Operation in Scaled Voltage Conditions. IEEE Computer Architecture Letters, 2018, 17, 109-112.	1.0	16
22	Analysis and Characterization of Ultra Low Power Branch Predictors. , 2018, , .		9
23	An energy-efficient and error-resilient server ecosystem exceeding conservative scaling limits. , 2018, , .		14
24	HealthLog Monitor: A Flexible System-Monitoring Linux Service. , 2018, , .		6
25	Measuring and Exploiting Guardbands of Server-Grade ARMv8 CPU Cores and DRAMs. , 2018, , .		18
26	Micro-Viruses for Fast System-Level Voltage Margins Characterization in Multicore CPUs. , 2018, , .		15
27	Multi-faceted microarchitecture level reliability characterization for NVIDIA and AMD GPUs. , 2018, , .		13
28	Performance-aware reliability assessment of heterogeneous chips. , 2017, , .		8
29	An Agile Post-Silicon Validation Methodology for the Address Translation Mechanisms of Modern Microprocessors. IEEE Transactions on Device and Materials Reliability, 2017, 17, 3-11.	1.5	2
30	Foreword to the Special Section on the IEEE International On-Line Testing and Robust System Design Symposium (IOLTS) 2016. IEEE Transactions on Device and Materials Reliability, 2017, 17, 1-2.	1.5	0
31	MeRLiN. , 2017, , .		33
32	Error-Resilient Server Ecosystems for Edge and Cloud Datacenters. Computer, 2017, 50, 78-81.	1.2	1
33	Harnessing voltage margins for energy efficiency in multicore CPUs. , 2017, , .		53
34	Microarchitecture level reliability comparison of modern GPU designs: First findings. , 2017, , .		4
35	Voltage margins identification on commercial x86-64 multicore microprocessors. , 2017, , .		20
36	RT Level vs. Microarchitecture-Level Reliability Assessment: Case Study on ARM(R) Cortex(R)-A9 CPU. , 2017, , .		20

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37	MeRLiN. Computer Architecture News, 2017, 45, 241-254.	2.5	4
38	Unveiling difficult bugs in address translation caching arrays for effective post-silicon validation. , 2016, , .		6
39	ISA-independent post-silicon validation for the address translation mechanisms of modern microprocessors. , 2016, , .		2
40	RIIF-2: Toward the next generation reliability information interchange format. , 2016, , .		2
41	Cross-layer system reliability assessment framework for hardware faults. , 2016, , .		20
42	Hierarchical Synthesis of Quantum and Reversible Architectures. International Journal of Parallel Programming, 2016, 44, 1028-1053.	1.1	0
43	Anatomy of microarchitecture-level reliability assessment: Throughput and accuracy. , 2016, , .		32
44	Faults in data prefetchers: Performance degradation and variability. , 2016, , .		2
45	Microprocessor reliability-performance tradeoffs assessment at the microarchitecture level. , 2016, , .		2
46	GUFI: A framework for GPUs reliability assessment. , 2016, , .		41
47	Accelerated microarchitectural Fault Injection-based reliability assessment. , 2015, , .		12
48	Efficient parallelization of the Discrete Wavelet Transform algorithm using memory-oblivious optimizations. , 2015, , .		0
49	Differential Fault Injection on Microarchitectural Simulators. , 2015, , .		63
50	Cross-layer reliability evaluation, moving from the hardware architecture to the system level: A CLERECO EU project overview. Microprocessors and Microsystems, 2015, 39, 1204-1214.	1.8	14
51	Dependable Multicore Architectures at Nanoscale: The View From Europe. IEEE Design and Test, 2015, 32, 17-28.	1.1	21
52	A Bayesian model for system level reliability estimation. , 2015, , .		1
53	Bayesian network early reliability evaluation analysis for both permanent and transient faults. , 2015, , .		2
54	Software-Based Self-Test for Small Caches in Microprocessors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1991-2004.	1.9	20

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55	Cross-Layer Early Reliability Evaluation for the Computing cOntinuum. , 2014, , .		1
56	Versatile architecture-level fault injection framework for reliability evaluation: A first report. , 2014, , .		9
57	Cross-layer early reliability evaluation: Challenges and promises. , 2014, , .		4
58	Power-aware optimization of software-based self-test for L1 caches in microprocessors. , 2014, , .		6
59	Accelerated online error detection in many-core microprocessor architectures. , 2014, , .		13
60	Combining checkpointing and scrubbing in FPGA-based real-time systems. , 2013, , .		19
61	The functional and performance tolerance of GPUs to permanent faults in registers. , 2013, , .		8
62	Online error detection in multiprocessor chips: A test scheduling study. , 2013, , .		4
63	Measuring the performance impact of permanent faults in modern microprocessor architectures. , 2013, , .		2
64	Reliability Challenges of Real-Time Systems in Forthcoming Technology Nodes. , 2013, , .		66
65	Software-Based Self Test Methodology for On-Line Testing of L1 Caches in Multithreaded Multicore Architectures. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 786-790.	2.1	18
66	Assessing the impact of hard faults in performance components of modern microprocessors. , 2013, , .		17
67	Deconfigurable microprocessor architectures for silicon debug acceleration. , 2013, , .		5
68	Deconfigurable microprocessor architectures for silicon debug acceleration. Computer Architecture News, 2013, 41, 631-642.	2.5	0
69	Accumulator Based 3-Weight Pattern Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 357-361.	2.1	17
70	Low Energy Online Self-Test of Embedded Processors in Dependable WSN Nodes. IEEE Transactions on Dependable and Secure Computing, 2012, 9, 86-100.	3.7	11
71	Efficient Memory Repair Using Cache-Based Redundancy. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2278-2288.	2.1	11
72	A Software-Based Self-Test methodology for on-line testing of data TLBs. , 2012, , .		7

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73	Chip Self-Organization and Fault Tolerance in Massively Defective Multicore Arrays. IEEE Transactions on Dependable and Secure Computing, 2011, 8, 207-217.	3.7	33
74	Architectures for online error detection and recovery in multicore processors. , 2011, , .		90
75	A Software-Based Self-Test methodology for on-line testing of processor caches. , 2011, , .		8
76	Guest Editors' Introduction: Special Section on Dependable Computer Architecture. IEEE Transactions on Computers, 2011, 60, 3-4.	2.4	1
77	Accelerating microprocessor silicon validation by exposing ISA diversity. , 2011, , .		27
78	Towards improved survivability in safety-critical systems. , 2011, , .		14
79	MT-SBST: Self-test optimization in multithreaded multicore architectures. , 2010, , .		17
80	Microprocessor Software-Based Self-Testing. IEEE Design and Test of Computers, 2010, 27, 4-19.	1.4	204
81	Recursive Pseudo-Exhaustive Two-Pattern Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 142-152.	2.1	12
82	A software-based self-test methodology for in-system testing of processor cache tag arrays. , 2010, , .		5
83	Energy optimal on-line Self-Test of microprocessors in WSN nodes. , 2010, , .		0
84	SBST for on-line detection of hard faults in multiprocessor applications under energy constraints. , 2010, , .		0
85	Exploiting Thread-Level Parallelism in Functional Self-Testing of CMT Processors. , 2009, , .		14
86	An Input Vector Monitoring Concurrent BIST scheme exploiting “X” values. , 2009, , .		4
87	Test Program Generation for Communication Peripherals in Processor-Based SoC Devices. IEEE Design and Test of Computers, 2009, 26, 52-63.	1.4	28
88	Online Periodic Self-Test Scheduling for Real-Time Processor-Based Systems Dependability Enhancement. IEEE Transactions on Dependable and Secure Computing, 2009, 6, 152-158.	3.7	15
89	Instruction-Based Online Periodic Self-Testing of Microprocessors with Floating-Point Units. IEEE Transactions on Dependable and Secure Computing, 2009, 6, 124-134.	3.7	10
90	Software-Based Self-Testing of Symmetric Shared-Memory Multiprocessors. IEEE Transactions on Computers, 2009, 58, 1682-1694.	2.4	35

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91	Hybrid-SBST Methodology for Efficient Testing of Processor Cores. IEEE Design and Test of Computers, 2008, 25, 64-75.	1.4	59
92	An Input Vector Monitoring Concurrent BIST Architecture Based on a Precomputed Test Set. IEEE Transactions on Computers, 2008, 57, 1012-1022.	2.4	29
93	Challenges in Scaling Software-Based Self-Testing to Multithreaded Chip Multiprocessors. , 2008, , .		0
94	Low Energy On-Line SBST of Embedded Processors. , 2008, , .		4
95	Systematic Software-Based Self-Test for Pipelined Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1441-1453.	2.1	79
96	Functional Self-Testing for Bus-Based Symmetric Multiprocessors. , 2008, , .		3
97	Selecting Power-Optimal SBST Routines for On-Line Processor Testing. Proceedings of the IEEE European Test Workshop, 2007, , .	0.0	4
98	Functional Processor-Based Testing of Communication Peripherals in Systems-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 971-975.	2.1	12
99	A methodology for detecting performance faults in microprocessors via performance monitoring hardware. , 2007, , .		30
100	Guest Editorial: Special Section on â€œAutonomous Silicon Validation and Testing of Microprocessors and Microprocessor-Based Systemsâ€• IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 493-494.	2.1	0
101	On-Line Periodic Self-Testing of High-Speed Floating-Point Units in Microprocessors. , 2007, , .		3
102	A Functional Self-Test Approach for Peripheral Cores in Processor-Based SoCs. , 2007, , .		7
103	Systematic software-based self-test for pipelined processors. , 2006, , .		32
104	Testability Analysis and Scalable Test Generation for High-Speed Floating-Point Units. IEEE Transactions on Computers, 2006, 55, 1449-1457.	2.4	4
105	Systematic software-based self-test for pipelined processors. Proceedings - Design Automation Conference, 2006, , .	0.0	8
106	A Concurrent Built-In Self-Test Architecture Based on a Self-Testing RAM. IEEE Transactions on Reliability, 2005, 54, 69-78.	3.5	33
107	Effective software-based self-test strategies for on-line periodic testing of embedded processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 88-99.	1.9	41
108	Software-Based Self-Testing of Embedded Processors. IEEE Transactions on Computers, 2005, 54, 461-475.	2.4	160

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109	Accumulator-based test generation for robust sequential fault testing in DSP cores in near-optimal time. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 1079-1086.	2.1	24
110	Accumulator-based weighted pattern generation. , 2005, , .		8
111	Accumulator-based built-in self-test generator for robustly detectable sequential fault testing. IEE Proceedings: Computers and Digital Techniques, 2004, 151, 466.	1.6	6
112	Embedded Processor-Based Self-Test. Frontiers in Electronic Testing, 2004, , .	0.3	36
113	Easily Testable Cellular Carry Lookahead Adders. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 285-298.	0.9	17
114	Instruction-Based Self-Testing of Processor Cores. Journal of Electronic Testing: Theory and Applications (JETTA), 2003, 19, 103-112.	0.9	30
115	An Effective Deterministic BIST Scheme for Shifter/Accumulator Pairs in Datapaths. Journal of Electronic Testing: Theory and Applications (JETTA), 2001, 17, 97-107.	0.9	3
116	Power-/energy-efficient BIST schemes for processor data paths. IEEE Design and Test of Computers, 2000, 17, 15-28.	1.4	15
117	Sequential fault modeling and test pattern generation for CMOS iterative logic arrays. IEEE Transactions on Computers, 2000, 49, 1083-1099.	2.4	22
118	An effective built-in self-test scheme for parallel multipliers. IEEE Transactions on Computers, 1999, 48, 936-950.	2.4	40
119	An effective BIST scheme for carry-save and carry-propagate array multipliers. , 0, , .		18
120	An effective BIST scheme for Booth multipliers. , 0, , .		15