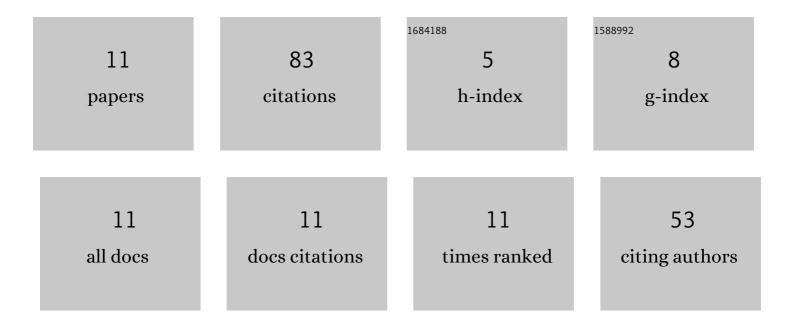
Siwan Dong

List of Publications by Year in descending order

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SIWAN DONG

#	Article	IF	CITATIONS
1	A 0.25-V 90ÂdB PVT-stabilized four-stage OTA with linear Q-factor modulation and fast slew-rate enhancement for ultra-low supply ADCs. AEU - International Journal of Electronics and Communications, 2022, 144, 154044.	2.9	5
2	A 0.6-V 12-bit 13.2-fJ/conversion-step SAR ADC with time-domain VCDL-based comparator and metastability immunity technique. Microelectronics Journal, 2022, 122, 105406.	2.0	3
3	A 0.3-V 8.72-nW OTA with Bulk-Driven Low-Impedance Compensation for Ultra-Low Power Applications. Circuits, Systems, and Signal Processing, 2021, 40, 2209-2227.	2.0	10
4	A three-stage OTA with transistor impendence modulation compensation for ultra-large load applications. Analog Integrated Circuits and Signal Processing, 2021, 108, 671-677.	1.4	0
5	A three-stage OTA with hybrid active miller enhanced compensation technique for large to heavy load applications. Microelectronics Journal, 2021, 115, 105199.	2.0	3
6	A chaos-based true random number generator based on OTA sharing and non-flipped folded Bernoulli mapping for high-precision ADC calibration. Microelectronics Journal, 2021, 116, 105259.	2.0	10
7	A 17.6-nW 35.7-ppm/ŰC Temperature Coefficient All-SVT-MOSFET Subthreshold Voltage Reference in Standard 0.18- <i>̼</i> m N-Well CMOS. IEEE Access, 2020, 8, 94043-94053.	4.2	3
8	A Reconfigurable Low Noise Amplifier with Sub-amplifier Compensation for Wearable Wireless Neural Recording System. , 2019, , .		5
9	A 10-Bit 120ÂkS/s SAR ADC Without Reset Energy for Biomedical Electronics. Circuits, Systems, and Signal Processing, 2019, 38, 5411-5425.	2.0	17
10	A transconductance-enhancement cascode Miller compensation for low-power multistage amplifiers. Microelectronics Journal, 2018, 73, 94-100.	2.0	20
11	A 0.6-V, 1.56-nW, 5.87-ppm/°C, 0.23%/V CMOS-Only Subthreshold Voltage Reference with the Threshold Voltage Difference, Circuits, Systems, and Signal Processing, 0, , 1.	2.0	7