Carlos Carreras Vaquer

List of Publications by Year
in descending order

43	309	1040056 9	940533 16
papers	citations	h-index	g-index

44	44	44	239
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Improved Interval-Based Characterization of Fixed-Point LTI Systems With Feedback Loops. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1923-1933.	2.7	41
2	Extension versus Bending for Continuum Robots. International Journal of Advanced Robotic Systems, 2006, 3, 26.	2.1	40
3	SQNR Estimation of Fixed-Point DSP Algorithms. Eurasip Journal on Advances in Signal Processing, 2010, 2010, .	1.7	28
4	Power Estimation of Embedded Multiplier Blocks in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 835-839.	3.1	26
5	Power Measurement Methodology for FPGA Devices. IEEE Transactions on Instrumentation and Measurement, 2011, 60, 237-247.	4.7	23
6	FPGA ACCELERATION FOR DNA SEQUENCE ALIGNMENT. Journal of Circuits, Systems and Computers, 2007, 16, 245-266.	1.5	20
7	Binary Division Power Models for High-Level Power Estimation of FPGA-Based DSP Circuits. IEEE Transactions on Industrial Informatics, 2014, 10, 393-398.	11.3	15
8	A complete dynamic power estimation model for data-paths in FPGA DSP designs. The Integration VLSI Journal, 2012, 45, 172-185.	2.1	14
9	Fast and accurate power estimation of FPGA DSP components based on high-level switching activity models. International Journal of Electronics, 2008, 95, 653-668.	1.4	11
10	High-Level Synthesis of Multiple Word-Length DSP Algorithms Using Heterogeneous-Resource FPGAs. , 2006, , .		10
11	Improved schemes for tracking residual frequency offset in DVB-T systems. IEEE Transactions on Consumer Electronics, 2010, 56, 415-422.	3.6	9
12	A Formal Method for Optimal High-Level Casting of Heterogeneous Fixed-Point Adders and Subtractors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 52-62.	2.7	9
13	Architectural Synthesis of Fixed-Point DSP Datapaths Using FPGAs. International Journal of Reconfigurable Computing, 2009, 2009, 1-14.	0.2	8
14	A Multistandard Frequency Offset Synchronization Scheme for 802.11n, 802.16d, LTE, and DVB-T/H Systems. Journal of Computer Systems, Networks, and Communications, 2010, 2010, 1-9.	1.2	7
15	Memory optimization in FPGA-accelerated scientific codes based on unstructured meshes. Journal of Systems Architecture, 2014, 60, 579-591.	4.3	6
16	A Methodology for CFD Acceleration Through Reconfigurable Hardware. , 2008, , .		5
17	Comparative Evaluation of Carrier Frequency Offset Tracking Schemes for WiMAX OFDM Systems. , 2007, , .		4
18	Power estimation of dividers implemented in FPGAs. , 2011, , .		4

#	Article	IF	Citations
19	Architectural synthesis of DSP circuits under simultaneous error and time constraints. , 2010, , .		3
20	Fast fixed-point optimization of DSP algorithms. , 2010, , .		3
21	A reduced complexity scheme for carrier frequency synchronization in uplink 802.16e OFDMA. Eurasip Journal on Advances in Signal Processing, 2012, 2012, .	1.7	3
22	High-Performance Decoding of Variable-Length Memory Data Packets for FPGA Stream Processing. , 2019, , .		3
23	Switching Activity Models for Power Estimation in FPGA Multipliers. , 2007, , 201-213.		3
24	A Comparison of Frequency Offset Synchronization Algorithms for WiMAX OFDM Systems. , 2007, , .		2
25	Mesh traversal and sorting for efficient memory usage in scientific codes. , 2011, , .		2
26	Fast Fixed-Point Optimization of DSP Algorithms. International Federation for Information Processing, 2012, , 182-205.	0.4	2
27	Optimized Architectural Synthesis of Fixed-Point Datapaths. , 2008, , .		1
28	A Practical Method for Testing High-Speed Networking Hardware Architectures. , 2009, , .		1
29	Turning control flow graphs into function calls: Code generation for heterogeneous architectures. , 2012, , .		1
30	Automated Timing Characterization of High-Performance Macroblocks for Latency Insensitive FPGA Designs. , 2018, , .		1
31	Grid-Based Histogram Arithmetic for the Probabilistic Analysis of Functions. Lecture Notes in Computer Science, 2000, , 107-123.	1.3	1
32	Floorplan-based FPGA interconnect power estimation in DSP circuits. , 2009, , .		1
33	Optimized Synthesis of DSP Cores Combining Logic-based and Embedded FPGA Resources. , 2006, , .		0
34	Adding Value to TCP/IP Based Information exchange Security by Specialized Hardware. , 2007, , .		0
35	A Comparison of Approaches for High-Level Power Estimation of LUT-Based DSP Components. , 2008, , .		0
36	Fast and accurate frequency offset tracking scheme for OFDM DVB-T standard. , 2010, , .		0

#	Article	IF	Citations
37	EVALUATION OF RAPID PROTOTYPING SOLUTIONS FOR A 802.16D FREQUENCY OFFSET ESTIMATION SCHEME. Journal of Circuits, Systems and Computers, 2012, 21, 1250056.	1.5	0
38	Witelo: Automated generation and timing characterization of distributed-control macroblocks for high-performance FPGA designs. The Integration VLSI Journal, 2019, 68, 1-11.	2.1	0
39	Behavioural Biometrics Hardware Based on Bioinformatics Matching. Advances in Intelligent and Soft Computing, 2009, , 171-178.	0.2	0
40	Applications of Interval-Based Simulations to the Analysis and Design of Digital LTI Systems. , 0, , .		0
41	Design and Implementation of Hardware Modules for Baseband Processing in Radio Transceivers. Advances in Wireless Technologies and Telecommunication Book Series, 2012, , 266-286.	0.4	0
42	Frequency Synchronization for OFDM/OFDMA Systems. Advances in Wireless Technologies and Telecommunication Book Series, 2012, , 216-236.	0.4	0
43	Analytic model of a Cache Only Memory Architecture. Lecture Notes in Computer Science, 1994, , 336-350.	1.3	0