Takashi Sato

List of Publications by Year
in descending order

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160	1,143	623734	713466
papers	citations	14 h-index	21 g-index

161	161	161	747
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Accelerating Parameter Extraction of Power MOSFET Models Using Automatic Differentiation. IEEE Transactions on Power Electronics, 2022, 37, 2970-2982.	7.9	3
2	Evaluation of thermal couple impedance model of power modules for accurate die temperature estimation up to 200 Â°C. Japanese Journal of Applied Physics, 2022, 61, SC1082.	1.5	1
3	Yield and leakage current of organic thin-film transistor logic gates toward reliable and low-power operation of large-scale logic circuits for IoT nodes. Japanese Journal of Applied Physics, 2022, 61, SC1044.	1.5	3
4	VisualNet: An End-to-End Human Visual System Inspired Framework to Reduce Inference Latency of Deep Neural Networks. IEEE Transactions on Computers, 2022, 71, 2717-2727.	3.4	1
5	Stable organic SRAM cell with p-type access transistors. Japanese Journal of Applied Physics, 2021, 60, SBBG04.	1.5	4
6	Separation of bias stress degradation between insulator and semiconductor carrier trapping in organic thin-film transistors. Japanese Journal of Applied Physics, 2021, 60, SBBG06.	1.5	2
7	An SRAM-based Scratchpad Memory for Organic IoT Sensors. , 2021, , .		1
8	APAS: Application-Specific Accelerators for RLWE-Based Homomorphic Linear Transformations. IEEE Transactions on Information Forensics and Security, 2021, 16, 4663-4678.	6.9	5
9	Privacy-Preserving Medical Image Segmentation via Hybrid Trusted Execution Environment. , 2021, , .		1
10	Dominant Model Parameter Extraction for Analyzing Current Imbalance in Parallel Connected SiC MOSFETs. , 2021, , .		3
11	Clustering Approach for Solving Traveling Salesman Problems via Ising Model Based Solver. , 2020, , .		10
12	ENSEI: Efficient Secure Inference via Frequency-Domain Homomorphic Convolution for Privacy-Preserving Visual Recognition. , 2020, , .		19
13	Measurement and Modeling of Ambient-Air-Induced Degradation in Organic Thin-Film Transistor. IEEE Transactions on Semiconductor Manufacturing, 2020, 33, 216-223.	1.7	4
14	Ed-PUF: Event-Driven Physical Unclonable Function for Camera Authentication in Reactive Monitoring System. IEEE Transactions on Information Forensics and Security, 2020, 15, 2824-2839.	6.9	14
15	Statistical Extraction of Normally and Lognormally Distributed Model Parameters for Power MOSFETs. IEEE Transactions on Semiconductor Manufacturing, 2020, 33, 150-158.	1.7	4
16	Recovery-aware bias-stress degradation model for organic thin-film transistors considering drain and gate bias voltages. Japanese Journal of Applied Physics, 2020, 59, SGGG08.	1.5	6
17	Organic Current Mirror PUF for Improved Stability Against Device Aging. IEEE Sensors Journal, 2020, 20, 7569-7578.	4.7	9
18	Influence of Device Parameter Variability on Current Sharing of Parallel-Connected SiC MOSFETs. , 2020, , .		2

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19	OCM-PUF: organic current mirror PUF with enhanced resilience to device degradation. , 2019, , .		5
20	A compact model of I -V characteristic degradation for organic thin film transistors. , 2019, , .		5
21	GPU-based Ising computing for solving max-cut combinatorial optimization problems. The Integration VLSI Journal, 2019, 69, 335-344.	2.1	19
22	Filianore. , 2019, , .		11
23	A study on statistical parameter modeling of power MOSFET model by principal component analysis. , 2019, , .		1
24	Feasibility of a low-power, low-voltage complementary organic thin film transistor buskeeper physical unclonable function. Japanese Journal of Applied Physics, 2019, 58, SBBG03.	1.5	7
25	Towards practical homomorphic email filtering. , 2019, , .		1
26	Parameter Extraction Procedure for Surface-Potential-Based SiC MOSFET Model. , 2019, , .		4
27	Heart Rate Estimation during Exercise from Photoplethysmographic Signals Using Convolutional Neural Network. , 2019, , .		0
28	Time-Dependent Degradation in Device Characteristics and Countermeasures by Design. , 2019, , 203-243.		0
29	Hardware-Accelerated Secured NaÃ¯ve Bayesian Filter Based on Partially Homomorphic Encryption. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2019, E102.A, 430-439.	0.3	0
30	DArL: Dynamic Parameter Adjustment for LWE-based Secure Inference. , 2019, , .		3
31	Efficient worst-case timing analysis of critical-path delay under workload-dependent aging degradation. , 2018, , .		2
32	Surface-Potential-Based Silicon Carbide Power MOSFET Model for Circuit Simulation. IEEE Transactions on Power Electronics, 2018, 33, 10774-10783.	7.9	23
33	Ising-PUF: A machine learning attack resistant PUF featuring lattice like arrangement of Arbiter-PUFs. , 2018, , .		17
34	Coin Flipping PUF: A Novel PUF With Improved Resistance Against Machine Learning Attacks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 602-606.	3.0	18
35	Mechanically and electrically robust metal-mask design for organic CMOS circuits. Japanese Journal of Applied Physics, 2018, 57, 04FL05.	1.5	6
36	PARHELIA: Particle Filter-Based Heart Rate Estimation From Photoplethysmographic Signals During Physical Exercise. IEEE Transactions on Biomedical Engineering, 2018, 65, 189-198.	4.2	37

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37	A study on NBTI-induced delay degradation considering stress frequency dependence. , 2018, , .		2
38	A Transient Approach for Input Capacitance Characterization of Power Devices. , 2018, , .		1
39	Area Efficient Annealing Processor for Ising Model without Random Number Generator. IEICE Transactions on Information and Systems, 2018, E101.D, 314-323.	0.7	17
40	A Plotter-Based Automatic Measurement and Statistical Characterization of Multiple Discrete Power Devices. , 2018, , .		2
41	An Experimental Design of Robust Current-mode Arbiter PUF using Organic Thin Film Transistors. , 2018, , .		0
42	Interpolation-Based Object Detection Using Motion Vectors for Embedded Real-time Tracking Systems. , 2018, , .		15
43	Measurement and Modeling of Frequency Degradation of an oTFT Ring Oscillator. , 2018, , .		3
44	Modeling of interelectrode parasitic elements of V-groove SiC MOSFET. Nonlinear Theory and Its Applications IEICE, 2018, 9, 344-357.	0.6	0
45	Enhancing the solution quality of hardware ising-model solver via parallel tempering. , 2018, , .		16
46	RRAM/CMOS-Hybrid Architecture of Annealing Processor for Fully Connected Ising Model. , 2018, , .		2
47	Efficient parameter-extraction of SPICE compact model through automatic differentiation. , 2018, , .		2
48	DWE. , 2018, , .		7
49	Efficient Mini-Batch Training on Memristor Neural Network Integrating Gradient Calculation and Weight Update. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2018, E101.A, 1092-1100.	0.3	1
50	MRO-PUF: Physically Unclonable Function with Enhanced Resistance against Machine Learning Attacks Utilizing Instantaneous Output of Ring Oscillator. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2018, E101.A, 1035-1044.	0.3	1
51	Scalable Device Array for Statistical Characterization of BTI-Related Parameters. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1455-1466.	3.1	4
52	Efficient circuit failure probability calculation along product lifetime considering device aging. , 2017, , .		2
53	Pattern based runtime voltage emergency prediction: An instruction-aware block sparse compressed sensing approach. , 2017, , .		1
54	RTN in Scaled Transistors for On-Chip Random Seed Generation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2248-2257.	3.1	17

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55	Comparative study of path selection and objective function in replacing NBTI mitigation logic. , 2017, , .		2
56	Measurement and modeling of gateâ€“drain capacitance of silicon carbide vertical double-diffused MOSFET. Japanese Journal of Applied Physics, 2017, 56, 04CR07.	1.5	14
57	LSTA. , 2017, , .		11
58	SCAM: Secured content addressable memory based on homomorphic encryption. , 2017, , .		6
59	Device identification from mixture of measurable characteristics. , 2017, , .		1
60	Input capacitance determination of power MOSFETs from switching trajectories. , 2017, , .		4
61	Identification and Application of Invariant Critical Paths under NBTI Degradation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 2797-2806.	0.3	0
62	Efficient Aging-Aware Failure Probability Estimation Using Augmented Reliability and Subset Simulation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 2807-2815.	0.3	0
63	Utilization of Path-Clustering in Efficient Stress-Control Gate Replacement for NBTI Mitigation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 1464-1472.	0.3	0
64	Workload-Aware Worst Path Analysis of Processor-Scale NBTI Degradation. , 2016, , .		12
65	Analysis of transient behavior of SiC power MOSFETs based on surface potential model and its application to boost converter. , 2016, , .		1
66	A circuit simulation model for V-groove SiC power MOSFET. , 2016, , .		4
67	Identifications of thermal equivalent circuit for power MOSFETs through in-situ channel temperature estimation. , 2016, , .		3
68	Approximated Prediction Strategy for Reducing Power Consumption of Convolutional Neural Network Processor. , 2016, , .		8
69	Efficient transistor-level timing yield estimation via line sampling. , 2016, , .		3
70	Path Clustering for Test Pattern Reduction of Variation-Aware Adaptive Path Delay Testing. Journal of Electronic Testing: Theory and Applications (JETTA), 2016, 32, 601-609.	1.2	1
71	A simulation model for SiC power MOSFET based on surface potential. , 2016, , .		17
72	Physically unclonable function using RTN-induced delay fluctuation in ring oscillators. , 2016, , .		4

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73	Nonlinear delay-table approach for full-chip NBTI degradation prediction. , 2016, , .		4
74	A high power curve tracer for characterizing full operational range of SiC power transistors. , 2016, , .		9
75	Runtime NBTI Mitigation for Processor Lifespan Extension via Selective Node Control. , 2016, , .		7
76	Fast Estimation of NBTI-Induced Delay Degradation Based on Signal Probability. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2016, E99.A, 1400-1409.	0.3	1
77	Efficient Aging-Aware SRAM Failure Probability Calculation via Particle Filter-Based Importance Sampling. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2016, E99.A, 1390-1399.	0.3	1
78	ECRIPSE: An Efficient Method for Calculating RTN-Induced Failure Probability of an SRAM Cell. , 2015, , .		0
79	An Error Correction Scheme through Time Redundancy for Enhancing Persistent Soft-Error Tolerance of CGRAs. IEICE Transactions on Electronics, 2015, E98.C, 741-750.	0.6	0
80	A quadrocopter automatic control contest as an example of interdisciplinary design education. , 2014, , .		17
81	BTIarray: A Time-Overlapping Transistor Array for Efficient Statistical Characterization of Bias Temperature Instability. IEEE Transactions on Device and Materials Reliability, 2014, 14, 833-843.	2.0	11
82	Sensorless estimation of global device-parameters based on F<inf>max</inf> testing. , 2014, , .		0
83	A scalable device array for statistical device-aging characterization. , 2014, , .		0
84	Variability in device degradations: Statistical observation of NBTI for 3996 transistors. , 2014, , .		18
85	Aging Statistics Based on Trapping/Detrapping: Compact Modeling and Silicon Validation. IEEE Transactions on Device and Materials Reliability, 2014, 14, 607-615.	2.0	23
86	A Variability-Aware Adaptive Test Flow for Test Quality Improvement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1056-1066.	2.7	16
87	Experimental validation of minimum operating-voltage-estimation for low supply voltage circuits. , 2014, , .		0
88	Preparation of yttrium iron garnet thin films by mist chemical vapor deposition method and their magneto-optical properties. Japanese Journal of Applied Physics, 2014, 53, 05FB17.	1.5	8
89	Automation of Model Parameter Estimation for Random Telegraph Noise. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 2383-2392.	0.3	2
90	Multilevel Reliability Simulation for IC Design. , 2014, , 719-749.		2

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91	Hypersphere Sampling for Accelerating High-Dimension and Low-Failure Probability Circuit-Yield Analysis. IEICE Transactions on Electronics, 2014, E97.C, 280-288.	0.6	1
92	IDDQ Outlier Screening through Two-Phase Approach: Clustering-Based Filtering and Estimation-Based Current-Threshold Determination. IEICE Transactions on Information and Systems, 2014, E97.D, 2095-2104.	0.7	0
93	State-Dependence of On-Chip Power Distribution Network Capacitance. IEICE Transactions on Electronics, 2014, E97.C, 77-84.	0.6	0
94	Realization of frequency-domain circuit analysis through random walk. , 2013, , .		0
95	A Cost-Effective Selective TMR for Heterogeneous Coarse-Grained Reconfigurable Architectures Based on DFG-Level Vulnerability Analysis. , 2013, , .		12
96	Compact Modeling of Statistical BTI Under Trapping/Detrapping. IEEE Transactions on Electron Devices, 2013, 60, 3645-3654.	3.0	67
97	Statistical simulation methods for circuit performance analysis. , 2013, , .		0
98	Multi-trap RTN parameter extraction based on Bayesian inference. , 2013, , .		6
99	Hot-Swapping Architecture with Back-biased Testing for Mitigation of Permanent Faults in Functional Unit Array. , 2013, , .		2
100	An adaptive current-threshold determination for IDDQ testing based on Bayesian process parameter estimation. , 2013, , .		2
101	High-speed DFG-level SEU vulnerability analysis for applying selective TMR to resource-constrained CGRA. , 2013, , .		2
102	Device-Parameter Estimation through IDDQ Signatures. IEICE Transactions on Information and Systems, 2013, E96.D, 303-313.	0.7	1
103	Parallel Acceleration Scheme for Monte Carlo Based SSTA Using Generalized STA Processing Element. IEICE Transactions on Electronics, 2013, E96.C, 473-481.	0.6	1
104	A Cost-Effective Selective TMR for Coarse-Grained Reconfigurable Architectures Based on DFG-Level Vulnerability Analysis. IEICE Transactions on Electronics, 2013, E96.C, 454-462.	0.6	3
105	Aging statistics based on trapping/detrapping: Silicon evidence, modeling and long-term prediction. , 2012, , .		31
106	Physics matters. , 2012, , .		42
107	Statistical aging under dynamic voltage scaling: A logarithmic model approach. , 2012, , .		12
108	A Bayesian-based process parameter estimation using IDDQ current signature. , 2012, , .		6

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109	Statistical observations of NBTI-induced threshold voltage shifts on small channel-area devices. , 2012, , .		5
110	The odd couple: Antiresonance control by two capacitors of unequal series resistances. , 2012, , .		0
111	Bayesian Estimation of Multi-Trap RTN Parameters Using Markov Chain Monte Carlo Method. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 2272-2283.	0.3	7
112	Power Distribution Network Optimization for Timing Improvement with Statistical Noise Model and Timing Analysis. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 2261-2271.	0.3	0
113	A Variability-Aware Energy-Minimization Strategy for Subthreshold Circuits. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2012, E95.A, 2242-2250.	0.3	2
114	A device array for efficient bias-temperature instability measurements. , 2011, , .		24
115	A fully pipelined implementation of Monte Carlo based SSTA on FPGAs. , 2011, , .		2
116	A design strategy for sub-threshold circuits considering energy-minimization and yield-maximization. , 2011, , .		1
117	Acceleration of random-walk-based linear circuit analysis using importance sampling. , 2011, , .		8
118	Linear Time Calculation of On-Chip Power Distribution Network Capacitance Considering State-Dependence. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 2409-2416.	0.3	2
119	A Universal Equivalent Circuit Model for Ceramic Capacitors. IEICE Transactions on Electronics, 2010, E93-C, 347-354.	0.6	0
120	Sequential importance sampling for low-probability and high-dimensional SRAM yield analysis. , 2010, , .		45
121	Scan based process parameter estimation through path-delay inequalities. , 2010, , .		0
122	Decomposition of drain-current variation into gain-factor and threshold voltage variations. , 2010, , .		0
123	Robust importance sampling for efficient SRAM yield analysis. , 2010, , .		18
124	Modeling the Overshooting Effect for CMOS Inverter Delay Analysis in Nanometer Technologies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 250-260.	2.7	39
125	Path clustering for adaptive test. , 2010, , .		10
126	Linear time calculation of state-dependent power distribution network capacitance. , 2010, , .		2

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127	Impact of Self-Heating in Wire Interconnection on Timing. IEICE Transactions on Electronics, 2010, E93-C, 388-392.	0.6	1
128	Reliability Evaluation Environment for Exploring Design Space of Coarse-Grained Reconfigurable Architectures. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 2524-2532.	0.3	5
129	A Time-Slicing Ring Oscillator for Capturing Time-Dependent Delay Degradation and Power Supply Voltage Fluctuation. IEICE Transactions on Electronics, 2010, E93-C, 324-331.	0.6	0
130	Interconnect Modeling: A Physical Design Perspective. IEEE Transactions on Electron Devices, 2009, 56, 1840-1851.	3.0	11
131	An Adaptive Test for Parametric Faults Based on Statistical Timing Information. , 2009, , .		12
132	On-die parameter extraction from path-delay measurements. , 2009, , .		20
133	Accurate Array-Based Measurement for Subthreshold-Current of MOS Transistors. IEEE Journal of Solid-State Circuits, 2009, 44, 2977-2986.	5.4	17
134	Physical design challenges to nano-CMOS circuits. IEICE Electronics Express, 2009, 6, 703-720.	0.8	6
135	Analytical Estimation of Path-Delay Variation for Multi-Threshold CMOS Circuits. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 1031-1038.	0.3	0
136	One-Shot Voltage-Measurement Circuit Utilizing Process Variation. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 1024-1030.	0.3	0
137	Improvement in Computational Accuracy of Output Transition Time Variation Considering Threshold Voltage Variations. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 990-997.	0.3	0
138	2-Port Modeling Technique for Surface-Mount Passive Components Using Partial Inductance Concept. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 976-982.	0.3	0
139	An Approach for Reducing Leakage Current Variation due to Manufacturing Variability. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 3016-3023.	0.3	2
140	Structural Evolution of Human Recombinant Î±B-Crystallin under UV Irradiation. Biomacromolecules, 2008, 9, 431-434.	5.4	7
141	On-chip differential and common mode voltage measurement using off-chip referenced twin probing. , 2008, , .		3
142	A MOS transistor array with pico-ampere order precision for accurate characterization of leakage current variation. , 2008, , .		4
143	Accurate parasitic inductance determination of a ceramic capacitor through 2-port measurements. , 2008, , .		3
144	Decoupling capacitance allocation for timing with statistical noise model and timing analysis. , 2008, , .		2

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145	Non-invasive direct probing for on-chip voltage measurement. , 2008, , .		0
146	Non-parametric statistical static timing analysis. , 2008, , .		10
147	Substrate-geometry aware 2-port modeling for surface-mount passive components. , 2008, , .		3
148	Adaptable wire-length distribution with tunable occupation probability. , 2007, , .		2
149	Improvement of power distribution network using correlation-based regression analysis. , 2007, , .		1
150	Validation of a Full-Chip Simulation Model for Supply Noise and Delay Dependence on Average Voltage Drop With On-Chip Delay Measurement. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 868-872.	2.2	31
151	A MOS Transistor-Array for Accurate Measurement of Subthreshold Leakage Variation. , 2007, , .		5
152	A Multi-Drop Transmission-Line Interconnect in Si LSI. , 2007, , .		2
153	Shape of Î±-crystallin analyzed by small-angle neutron scattering. Journal of Applied Crystallography, 2007, 40, s200-s204.	4.5	5
154	Thermal Driven Module Placement Using Sequence-pair. , 2006, , .		2
155	A Time-Slicing Ring Oscillator for Capturing Instantaneous Delay Degradation and Power Supply Voltage Drop. , 2006, , .		11
156	Measurement results of delay degradation due to power supply noise well correlated with full-chip simulation. , 2006, , .		2
157	Timing analysis considering temporal supply voltage fluctuation. , 2005, , .		26
158	Probabilistic Crosstalk Delay Estimation for ASICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 1377-1383.	2.7	9
159	Accurate in situ measurement of peak noise and delay change induced by interconnect coupling. IEEE Journal of Solid-State Circuits, 2001, 36, 1587-1591.	5.4	20
160	A 5-GByte/s data-transfer scheme with bit-to-bit skew control for synchronous DRAM. IEEE Journal of Solid-State Circuits, 1999, 34, 653-660.	5.4	14