Niraj K Jha

List of Publications by Year
in descending order

128	4,123	201385	182168
papers	citations	27 h-index	51 g-index

128	128	128	3320
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	TUTOR: Training Neural Networks Using Decision Rules as Model Priors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 483-496.	1.9	1
2	SPRING: A Sparsity-Aware Reduced-Precision Monolithic 3D CNN Accelerator Architecture for Training and Inference. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 237-249.	3.2	12
3	GRAVITAS: Graphical Reticulated Attack Vectors for Internet-of-Things Aggregate Security. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 1331-1348.	3.2	5
4	SCANN: Synthesis of Compact and Accurate Neural Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3012-3025.	1.9	12
5	Incremental Learning Using a Grow-and-Prune Paradigm With Efficient Neural Networks. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 752-762.	3.2	15
6	Fast Design Space Exploration of Nonlinear Systems: Part II. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2984-2999.	1.9	3
7	CURIOUS: Efficient Neural Architecture Search Based on a Performance Predictor and Evolutionary Search. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 4975-4990.	1.9	2
8	Machine Learning Assisted Security Analysis of 5G-Network-Connected Systems. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 2006-2024.	3.2	10
9	MHDeep: Mental Health Disorder Detection System Based on Wearable Sensors and Artificial Neural Networks. Transactions on Embedded Computing Systems, 2022, 21, 1-22.	2.1	14
10	DiabDeep: Pervasive Diabetes Diagnosis Based on Wearable Medical Sensors and Efficient Neural Networks. IEEE Transactions on Emerging Topics in Computing, 2021, 9, 1139-1150.	3.2	17
11	YSUY: Your Smartphone Understands Youâ€"Using Machine Learning to Address Fundamental Human Needs. IEEE Transactions on Systems, Man, and Cybernetics: Systems, 2021, 51, 7553-7568.	5.9	4
12	SECRET: Semantically Enhanced Classification of Real-World Tasks. IEEE Transactions on Computers, 2021, 70, 440-456.	2.4	1
13	Software-Defined Design Space Exploration for an Efficient DNN Accelerator Architecture. IEEE Transactions on Computers, 2021, 70, 45-56.	2.4	12
14	Fully Dynamic Inference with Deep Neural Networks. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	13
15	SHARKS: Smart Hacking Approaches for RisK Scanning in Internet-of-Things and Cyber-Physical Systems based on Machine learning. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	10
16	Convolutional Autoencoder-Based Transfer Learning for Multi-Task Image Inferences. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	7
17	Towards Execution-Efficient LSTMs via Hardware-Guided Grow-and-Prune Paradigm. IEEE Transactions on Emerging Topics in Computing, 2021, , 1-1.	3.2	0
18	CovidDeep: SARS-CoV-2/COVID-19 Test Based on Wearable Medical Sensors and Efficient Neural Networks. IEEE Transactions on Consumer Electronics, 2021, 67, 244-256.	3.0	39

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19	Grow and Prune Compact, Fast, and Accurate LSTMs. IEEE Transactions on Computers, 2020, 69, 441-452.	2.4	44
20	McPAT-Monolithic: An Area/Power/Timing Architecture Modeling Framework for 3-D Hybrid Monolithic Multicore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2146-2156.	2.1	11
21	NeST: A Neural Network Synthesis Tool Based on a Grow-and-Prune Paradigm. IEEE Transactions on Computers, 2019, 68, 1487-1497.	2.4	108
22	ChamNet: Towards Efficient Network Design Through Platform-Aware Model Adaptation. , 2019, , .		146
23	Three-Dimensional Monolithic FinFET-Based 8T SRAM Cell Design for Enhanced Read Time and Low Leakage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 899-912.	2.1	13
24	Smart healthcare. , 2018, , .		5
25	OpSecure: A Secure Unidirectional Optical Channel for Implantable Medical Devices. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 410-419.	2.5	6
26	A Hierarchical Inference Model for Internet-of-Things. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 260-271.	2.5	17
27	PinMe: Tracking a Smartphone User around the World. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 420-435.	2.5	25
28	Genetic Programming for Energy-Efficient and Energy-Scalable Approximate Feature Computation in Embedded Inference Systems. IEEE Transactions on Computers, 2018, 67, 222-236.	2.4	9
29	A Monolithic 3D Hybrid Architecture for Energy-Efficient Computation. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 533-547.	2.5	9
30	Simultaneously ensuring smartness, security, and energy efficiency in Internet-of-Things sensors. , 2018, , .		9
31	Smart, Secure, Yet Energy-Efficient, Internet-of-Things Sensors. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 914-930.	2.5	40
32	Hybrid Monolithic 3-D IC Floorplanner. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1868-1880.	2.1	8
33	Smart Healthcare. Foundations and Trends in Electronic Design Automation, 2018, 12, 401-166.	1.0	25
34	Energy-Efficient Monolithic Three-Dimensional On-Chip Memory Architectures. IEEE Nanotechnology Magazine, 2018, 17, 620-633.	1.1	15
35	Improving Convergence and Simulation Time of Quantum Hydrodynamic Simulation: Application to Extraction of Best 10-nm FinFET Parameter Values. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 319-329.	2.1	5
36	Wearable Medical Sensor-Based System Design: A Survey. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 124-138.	2.5	104

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37	Keep the Stress Away with SoDA: Stress Detection and Alleviation System. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 269-282.	2.5	97
38	A Health Decision Support System for Disease Diagnosis Based on Wearable Medical Sensors and Machine Learning Ensembles. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 228-241.	2.5	84
39	A heterogeneous microprocessor for energy-scalable sensor inference using genetic programming. , 2017, , .		3
40	Using a Device State Library to Boost the Performance of TCAD Mixed-Mode Simulation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2616-2624.	2.1	1
41	Automated Quantum Circuit Synthesis and Cost Estimation for the Binary Welded Tree Oracle. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-14.	1.8	5
42	DISASTER: Dedicated Intelligent Security Attacks on Sensor-Triggered Emergency Responses. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 255-268.	2.5	9
43	CABA: Continuous Authentication Based on BioAura. IEEE Transactions on Computers, 2017, 66, 759-772.	2.4	48
44	A Comprehensive Study of Security of Internet-of-Things. IEEE Transactions on Emerging Topics in Computing, 2017, 5, 586-602.	3.2	464
45	Analytical Modeling of the SMART NoC. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 242-254.	2.5	3
46	Ultra-High Density Monolithic 3-D FinFET SRAM With Enhanced Read Stability. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1176-1187.	3.5	14
47	Physiological Information Leakage: A New Frontier in Health Information Security. IEEE Transactions on Emerging Topics in Computing, 2016, 4, 321-334.	3.2	30
48	A 3-D CPU-FPGA-DRAM Hybrid Architecture for Low-Power Computation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1649-1662.	2.1	11
49	GenFin: Genetic Algorithm-Based Multiobjective Statistical Logic Circuit Optimization Using Incremental Statistical Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1126-1139.	2.1	13
50	TCAD-Assisted Capacitance Extraction of FinFET SRAM and Logic Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 329-333.	2.1	3
51	Energy-Efficient Long-term Continuous Personal Health Monitoring. IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 85-98.	2.5	78
52	Design of Efficient Content Addressable Memories in High-Performance FinFET Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 963-967.	2.1	16
53	FDR 2.0: A Low-Power Dynamically Reconfigurable Architecture and Its FinFET Implementation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1987-2000.	2.1	7
54	Vibration-based secure side channel for medical devices. , 2015, , .		35

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55	Signal Processing With Direct Computations on Compressively Sensed Data. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 30-43.	2.1	34
56	PAQCS: Physical Design-Aware Fault-Tolerant Quantum Circuit Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1221-1234.	2.1	47
57	FinFETs: From Devices to Architectures. Advances in Electronics, 2014, 2014, 1-21.	1.9	137
58	Trustworthiness of Medical Devices and Body Area Networks. Proceedings of the IEEE, 2014, 102, 1174-1188.	16.4	95
59	FinPrin: FinFET Logic Circuit Analysis and Optimization Under PVT Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2462-2475.	2.1	25
60	TCAD structure synthesis and capacitance extraction of a voltage-controlled oscillator using automated layout-to-device synthesis methodology. , 2014, , .		1
61	FTQLS: Fault-Tolerant Quantum Logic Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1350-1363.	2.1	23
62	FinCANON: A PVT-Aware Integrated Delay and Power Modeling Framework for FinFET-Based Caches and On-Chip Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1150-1163.	2.1	21
63	A Fine-Grain Dynamically Reconfigurable Architecture Aimed at Reducing the FPGA-ASIC Gaps. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2607-2620.	2.1	18
64	A defense framework against malware and vulnerability exploits. International Journal of Information Security, 2014, 13, 439-452.	2.3	10
65	FinFET Logic Circuit Optimization with Different FinFET Styles: Lower Power Possible at Higher Supply Voltage. , 2014, , .		6
66	Fin Prin: Analysis and Optimization of FinFET Logic Circuits under PVT Variations. , 2013, , .		2
67	Design of Logic Gates and Flip-Flops in High-Performance FinFET Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1975-1988.	2.1	57
68	Localized Heating for Building Energy Efficiency. , 2013, , .		3
69	Algorithm-Driven Architectural Design Space Exploration of Domain-Specific Medical-Sensor Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1849-1862.	2.1	11
70	Variable-Pipeline-Stage Router. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1669-1682.	2.1	8
71	Improving the Trustworthiness of Medical Device Software with Formal Verification Methods. IEEE Embedded Systems Letters, 2013, 5, 50-53.	1.3	33
72	Optimized Quantum Gate Library for Various Physical Machine Descriptions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2055-2068.	2.1	18

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73	Efficient Methodologies for 3-D TCAD Modeling of Emerging Devices and Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 47-58.	1.9	15
74	3-D-TCAD-Based Parasitic Capacitance Extraction for Emerging Multigate Devices and Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 2094-2105.	2.1	49
75	MedMon: Securing Medical Devices Through Wireless Monitoring and Anomaly Detection. IEEE Transactions on Biomedical Circuits and Systems, 2013, 7, 871-881.	2.7	174
76	Emerging Frontiers in Embedded Security. , 2013, , .		24
77	Energy-efficient and Secure Sensor Data Transmission Using Encompression. , 2013, , .		18
78	Making buildings energy-efficient through retrofits: A survey of available technologies. , 2013, , .		8
79	Fault Models for Logic Circuits in the Multigate Era. IEEE Nanotechnology Magazine, 2012, 11, 182-193.	1.1	26
80	Design of Quantum Circuits for Random Walk Algorithms. , 2012, , .		4
81	SRAM-Based NATURE: A Dynamically Reconfigurable FPGA Based on 10T Low-Power SRAMs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2151-2156.	2.1	14
82	A Trusted Virtual Machine in an Untrusted Management Environment. IEEE Transactions on Services Computing, 2012, 5, 472-483.	3.2	45
83	Design of ultra-low-leakage logic gates and flip-flops in high-performance FinFET technology. , 2011, , .		22
84	Editorial - Announcing a New Editor-in-Chief. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 173-174.	2.1	0
85	Editorial : New Associate Editor Appointments. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 345-346.	2.1	0
86	Fault modeling for FinFET circuits. , 2010, , .		30
87	NanoV: Nanowire-based VLSI design. , 2010, , .		0
88	Low-power 3D nano/CMOS hybrid dynamically reconfigurable architecture. ACM Journal on Emerging Technologies in Computing Systems, 2010, 6, 1-32.	1.8	11
89	An evaluation of energy-saving technologies for residential purposes. , 2010, , .		14
90	Low-power FinFET circuit synthesis using surface orientation optimization. , 2010, , .		17

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91	Low-Power FinFET design schemes for NOR address decoders. , 2010, , .		6
92	Die-level leakage power analysis of FinFET circuits considering process variations. , 2010, , .		21
93	Fast Enhancement of Validation Test Sets for Improving the Stuck-at Fault Coverage of RTL Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 697-708.	2.1	1
94	In-Network Snoop Ordering (INSO): Snoopy coherence on unordered interconnects. , 2009, , .		45
95	Thermal characterization of BIST, scan design and sequential test methodologies. , 2009, , .		1
96	Pragmatic design of gated-diode FinFET DRAMs. , 2009, , .		7
97	GARNET: A detailed on-chip network model inside a full-system simulator. , 2009, , .		522
98	FinFET-based dynamic power management of on-chip interconnection networks through adaptive back-gate biasing. , 2009, , .		13
99	Editorial Appointments for the 2009-2010 Term. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 453-469.	2.1	0
100	Evaluation of multiple supply and threshold voltages for low-power FinFET circuit synthesis. , 2008, , .		4
101	A system-level perspective for efficient NoC design. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	6
102	System-Level Dynamic Thermal Management for High-Performance Microprocessors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 96-108.	1.9	131
103	Variability-Tolerant Register-Transfer Level Synthesis. , 2008, , .		4
104	Automatic Test Generation for Combinational Threshold Logic Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1035-1045.	2.1	13
105	Token flow control. , 2008, , .		73
106	Threshold Voltage Control through Multiple Supply Voltages for Power-Efficient FinFET Interconnects. , 2008, , .		12
107	What is majority/minority network synthesis?. ACM SIGDA Newsletter, 2008, 38, 1-1.	0.0	0
108	What is majority/minority network synthesis?. ACM SIGDA Newsletter, 2008, 38, 1-1.	0.0	0

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109	Generation of Heterogeneous Distributed Architectures for Memory-Intensive Applications Through High-Level Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1191-1204.	2.1	27
110	Hybrid Architectures for Efficient and Secure Face Authentication in Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 296-308.	2.1	7
111	SLOPES: Hardwareâ€“Software Cosynthesis of Low-Power Real-Time Distributed Embedded Systems With Dynamically Reconfigurable FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 508-526.	1.9	36
112	Automated Energy/Performance Macromodeling of Embedded Software. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 542-552.	1.9	15
113	Majority and Minority Network Synthesis With Application to QCA-, SET-, and TPL-Based Nanotechnologies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1233-1245.	1.9	46
114	Efficient Design for Testability Solution Based on Unsatisfiability for Register-Transfer Level Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1339-1345.	1.9	2
115	Hybrid Simulation for Energy Estimation of Embedded Software. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1843-1854.	1.9	16
116	A Synthesis Methodology for Hybrid Custom Instruction and Coprocessor Generation for Extensible Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 2035-2045.	1.9	22
117	Power-Efficient Scheduling for Heterogeneous Distributed Real-Time Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1161-1170.	1.9	46
118	CMOS logic design with independent-gate FinFETs. , 2007, , .		88
119	Architectural Support for Run-Time Validation of Program Data Properties. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 546-559.	2.1	16
120	Satisfiability-Based Automatic Test Program Generation and Design for Testability for Microprocessors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 518-530.	2.1	19
121	A Test Generation Framework for Quantum Cellular Automata Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 24-36.	2.1	47
122	Configuration and Extension of Embedded Processors to Optimize IPSec Protocol Execution. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 605-609.	2.1	7
123	Aiding Side-Channel Attacks on Cryptographic Software With Satisfiability-Based Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 465-470.	2.1	15
124	Simultaneous Dynamic Voltage Scaling of Processors and Communication Links in Real-Time Distributed Embedded Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 427-437.	2.1	40
125	Hardware-Assisted Run-Time Monitoring for Secure Program Execution on Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1295-1308.	2.1	66
126	A Scalable Synthesis Methodology for Application-Specific Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 1175-1188.	2.1	28

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127	Design of Algorithm-Based Fault Tolerant Systems with In-System Checks. , 1993, , .		4
128	Simultaneous dynamic voltage scaling of processors and communication links in real-time distributed embedded systems. , 0, , .		0