Tetsuya Iizuka

List of Publications by Year
in descending order

114 papers	465 citations	1040056 9 h-index	940533 16 g-index
114 all docs	114 docs citations	114 times ranked	275 citing authors

#	Article	IF	Citations
1	High-Precision Sub-Nyquist Sampling System Based on Modulated Wideband Converter for Communication Device Testing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 378-388.	5.4	8
2	Fully Dynamic Discrete-Time Î”Î£ ADC Using Closed-Loop Two-Stage Cascoded Floating Inverter Amplifiers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 944-948.	3.0	10
3	Analysis of strong-arm comparator with auxiliary pair for offset calibration. Analog Integrated Circuits and Signal Processing, 2022, 110, 535-546.	1.4	0
4	An ultra-compact leaky integrate-and-fire neuron with long and tunable time constant utilizing pseudo resistors for spiking neural networks. Japanese Journal of Applied Physics, 2022, 61, SC1051.	1.5	4
5	Analysis and simulation of MOSFET-based gate-voltage-independent capacitor. Japanese Journal of Applied Physics, 2022, 61, 064501.	1.5	2
6	4-Cycle-Start-Up Reference-Clock-Less Digital CDR Utilizing TDC-Based Initial Frequency Error Detection with Frequency Tracking Loop. IEICE Transactions on Electronics, 2022, , .	0.6	0
7	A Tutorial on Systematic Design of CMOS A/D Converters: Illustrated by a 10 b, 500 MS/s SAR ADC with 2 GHz RBW. , 2021, , .		4
8	An All-Standard-Cell-Based Synthesizable SAR ADC With Nonlinearity-Compensated RDAC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 2153-2162.	3.1	7
9	Shock-wave Transceiver Integration for Mm-wave Active Sensing Applications : Invited Paper. , 2021, , .		0
10	Theoretical Analysis of Noise Figure for Modulated Wideband Converter. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 298-308.	5.4	8
11	A 3.2-to-3.8GHz Calibration-Free Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving â€“66dBc Worst-Case In-Band Fractional Spur. , 2020, , .		4
12	A 140-GHz 14-dBm Power Amplifier using Power Combiner based on Symmetric Balun in 65-nm Bulk CMOS. , 2020, , .		2
13	A 40Ânm 16ÂGb/s differential transmitter with far-end crosstalk cancellation using injection timing control for high-density flexible flat cables. Analog Integrated Circuits and Signal Processing, 2020, 105, 191-202.	1.4	0
14	A Calibration Technique for Simultaneous Estimation of Actual Sensing Matrix Coefficients on Modulated Wideband Converters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 5561-5573.	5.4	10
15	A 3.2-to-3.8 GHz Harmonic-Mixer-Based Dual-Feedback Fractional-N PLL Achieving -65 dBc In-Band Fractional Spur. IEEE Solid-State Circuits Letters, 2020, 3, 534-537.	2.0	7
16	11â€…Gb/s 140â€…GHz OOK modulator with 24.6â€…dB isolation utilising cascaded switch and amplifierâ€based stages in 65â€…nm bulk CMOS. IET Circuits, Devices and Systems, 2020, 14, 322-326.	1.4	2
17	Theoretical Analysis on Noise Performance of Modulated Wideband Converters for Analog Testing. , 2020, , .		1
18	IEEE SSCS Japan Chapter Holds DL Program [Chapters]. IEEE Solid-State Circuits Magazine, 2019, 11, 64-64.	0.4	0

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19	IEEE SSCS Japan Chapter Holds A-SSCC 2018 Technical Seminar and DL Program [Chapters]. IEEE Solid-State Circuits Magazine, 2019, 11, 121-121.	0.4	0
20	A compact quick-start sub-mW pulse-width-controlled PLL with automated layout synthesis using a place-and-route tool. IEICE Electronics Express, 2019, 16, 20190546-20190546.	0.8	0
21	A 65Ânm CMOS Synthesizable Digital Low-Dropout Regulator Based on Voltage-to-Time Conversion with 99.6% Current Efficiency at 10-mA Load. IFIP Advances in Information and Communication Technology, 2019, , 1-13.	0.7	1
22	A 140 GHz area-and-power-efficient VCO using frequency doubler in 65 nm CMOS. IEICE Electronics Express, 2019, 16, 20190051-20190051.	0.8	3
23	A 0.0053-mm² 6-bit Fully-Standard-Cell-Based Synthesizable SAR ADC in 65 nm CMOS. , 2019, , .		9
24	Fault Detection of VLSI Power Supply Network Based on Current Estimation From Surface Magnetic Field. IEEE Transactions on Instrumentation and Measurement, 2019, 68, 2519-2530.	4.7	11
25	A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18-<inline-formula> <tex-math notation="LaTeX">mu </tex-math> </inline-formula>m CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 11-19.	3.1	21
26	Spatial resolution improvement for point light source detection in scintillator cube using SPAD array with multi pinholes. IEICE Electronics Express, 2019, 16, 20190390-20190390.	0.8	1
27	Noninvasive Localization of IGBT Faults by High-Sensitivity Magnetic Probe With RF Stimulation. IEEE Transactions on Instrumentation and Measurement, 2018, 67, 745-753.	4.7	21
28	Comprehensive Analysis of Distortion in the Passive FET Sample-and-Hold Circuit. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1157-1173.	5.4	19
29	A Synthesizable Digital Low-Dropout Regulator Based on Voltage-to-Time Conversion. , 2018, , .		5
30	A Consideration on LUT Linearization of Stochastic ADC in Sub-Ranging Architecture. , 2018, , .		0
31	IEEE SSCS Japan Chapter Hosts DL Prof. Hyeon-Min Bae [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 71-71.	0.4	0
32	IEEE DL Jun Ohta Presents Lecture at SSCS Japan Chapter [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 62-62.	0.4	0
33	Japan Chapter Holds ISSCC 2018 Technical Seminar [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 76-76.	0.4	0
34	DL Ali Sheikholeslami Visits the IEEE SSCS Japan Chapter [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 87-87.	0.4	0
35	Japan Chapter Hosts SSCS DL Prof. Yong Ping Xu [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 86-86.	0.4	0
36	SSCS Japan Chapter Holds DL Program [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 104-104.	0.4	0

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37	UCLA Professor Asad A. Abidi Visits SSCS Japan Chapter [Chapters]. IEEE Solid-State Circuits Magazine, 2018, 10, 92-92.	0.4	0
38	Time-Domain Approach for Analog Circuits: Fine-Resolution TDC and Quick-Start CDR Circuits. , 2018, , .		1
39	A Unified Analysis of the Signal Transfer Characteristics of a Single-Path FET-R-C Circuit. IEICE Transactions on Electronics, 2018, E101.C, 432-443.	0.6	1
40	Optimal Design Method of Sub-Ranging ADC Based on Stochastic Comparator. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2018, E101.A, 410-424.	0.3	2
41	Quick-Start Pulse Width Controlled PLL with Frequency and Phase Presetting. IEICE Transactions on Electronics, 2018, E101.C, 218-223.	0.6	1
42	Time-domain approach for analog circuits in deep sub-micron LSI. IEICE Electronics Express, 2018, 15, 20182001-20182001.	0.8	16
43	Analysis and design of impulse signal generator based on current-mode excitation and transmission line resonator. Analog Integrated Circuits and Signal Processing, 2018, 97, 457-470.	1.4	0
44	Digitally-Controlled Compensation Current Injection to ATE Power Supply for Emulation of Customer Environment. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 147-161.	1.2	0
45	Triangular Active Charge Injection Method for Resonant Power Supply Noise Reduction. IEICE Transactions on Electronics, 2018, E101.C, 292-298.	0.6	0
46	A 15 Ã— 15 SPAD array sensor with breakdown-pixel-extraction architecture for efficient data readout. , 2017, , .		0
47	CMOS-on-quartz pulse generator for low power applications. , 2017, , .		0
48	Experimental demonstration of non-destructive detection of IGBT fault positions by magnetic sensor. , 2017, , .		5
49	Analysis of VLSI power supply network based on current estimation through magnetic field measurement. , 2017, , .		2
50	Extension of power supply impedance emulation method on ATE for multiple power domain. , 2017, , .		0
51	Session 4 â€" Modeling and measurement of mixed-signal circuits. , 2017, , .		0
52	A 40-kS/s 16-bit non-binary SAR ADC in 0.18 CMOS with noise-tunable comparator. , 2017, , .		1
53	High-sensitivity micro-magnetic probe for the applications of safety and security. , 2017, , .		2
54	Japan Chapter Holds VLSI Symposium on Circuits Technical Seminar and Distinguished Lecturer Program [Chapters]. IEEE Solid-State Circuits Magazine, 2017, 9, 118-118.	0.4	0

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55	A SPAD array sensor based on breakdown pixel extraction architecture with background readout for scintillation detector. , 2017, , .		3
56	High Spatial Resolution Detection Method for Point Light Source in Scintillator. IS&T International Symposium on Electronic Imaging, 2017, 29, 18-23.	0.4	2
57	An ultra-wide-range fine-resolution two-step time-to-digital converter with built-in foreground coarse gain calibration. , 2017, , .		1
58	A triangular active charge injection scheme using a resistive current for resonant power supply noise suppression. , 2017, , .		1
59	Impulse signal generator based on current-mode excitation and transmission line resonator. , 2017, , .		3
60	Design, Analysis and Implementation of Pulse Generator by CMOS Flipped on Glass for Low Power UWB-IR. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 200-209.	0.3	1
61	A Gate Delay Mismatch Tolerant Time-Mode Analog Accumulator Using a Delay Line Ring. IEICE Transactions on Electronics, 2017, E100.C, 736-745.	0.6	0
62	A PLL Compiler from Specification to GDSII. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2017, E100.A, 2741-2749.	0.3	1
63	A 15 Ã— 15 single photon avalanche diode sensor featuring breakdown pixels extraction architecture for efficient data readout. Japanese Journal of Applied Physics, 2016, 55, 04EF04.	1.5	3
64	Analysis and implementation of quick-start pulse generator by CMOS flipped on quartz substrate. , 2016, , .		5
65	A fine-resolution pulse-shrinking time-to-digital converter with completion detection utilizing built-in offset pulse. , 2016, , .		9
66	Experimental demonstration of stochastic comparators for fine resolution ADC without calibration. , 2016, , .		2
67	Resonant power supply noise reduction using a triangular active charge injection. , 2016, , .		1
68	Common pitfalls in application of a threshold detection comparator to a continuous-time level crossing quantization. , 2016, , .		1
69	Power supply impedance emulation to eliminate overkills and underkills due to the impedance difference between ATE and customer board. , 2016, , .		3
70	FET-R-C Circuits: A Unified Treatmentâ€"Part I: Signal Transfer Characteristics of a Single-Path. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1325-1336.	5.4	30
71	FET-R-C Circuits: A Unified Treatmentâ€"Part II: Extension to Multi-Paths, Noise Figure, and Driving-Point Impedance. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1337-1348.	5.4	30
72	A 4-cycle-start-up reference-clock-less all-digital burst-mode CDR based on cycle-lock gated-oscillator with frequency tracking. , 2016, , .		5

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73	A damping pulse generator based on regenerated trigger switch. , 2016, , .		4
74	An Asynchronous Summation Circuit for Noise Filtering in Single Photon Avalanche Diode Sensors. Journal of Circuits, Systems and Computers, 2016, 25, 1640017.	1.5	1
75	Analytical Design Optimization of Sub-ranging ADC Based on Stochastic Comparator. , 2016, , .		0
76	An Asynchronous Projection and Summation Circuit for In-Pixel Processing in Single Photon Avalanche Diode Sensors. , 2015, , .		1
77	Tracking PVT variations of Pulse Width Controlled PLL using variable-length ring oscillator. , 2015, , .		2
78	Spacial Resolution Enhancement for Integrated Magnetic Probe by Two-Step Removal of Si-Substrate Beneath the Coil. IEEE Transactions on Magnetics, 2015, 51, 1-4.	2.1	5
79	Session 3 — Optical interconnect and reliability enhancement techniques. , 2015, , .		0
80	Session 12 — Tutorial — beyond CMOS: Large area electronics-concepts and prospects. , 2015, , .		0
81	A calibration-free time difference accumulator using two pulses propagating on a single buffer ring. , 2015, , .		1
82	A Near-Field Magnetic Sensing System With High-Spatial Resolution and Application for Security of Cryptographic LSIs. IEEE Transactions on Instrumentation and Measurement, 2015, 64, 840-848.	4.7	15
83	F1: High-speed interleaved ADCs. , 2015, , .		0
84	Embedded tutorial: Test and manufacturability for silicon photonics and 3D integration. , 2014, , .		0
85	High-resolution measurement of magnetic field generated from cryptographic LSIs. , 2014, , .		1
86	A Structured Routing Architecture for Practical Application of Character Projection Method in Electron-Beam Direct Writing. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2014, E97.A, 1688-1698.	0.3	3
87	A Pulse Width controlled PLL and its automated design flow. , 2013, , .		5
88	An all-digital time difference hold-and-replication circuit utilizing a dual pulse ring oscillator. , 2013, , .		0
89	An Integrated High-Precision Probe System in 0.18-$mu{m m}$ CMOS for Near-Field Magnetic Measurements on Cryptographic LSIs. IEEE Sensors Journal, 2013, 13, 2675-2682.	4.7	22
90	A true 4-cycle lock reference-less all-digital burst-mode CDR utilizing coarse-fine phase generator with embedded TDC. , 2013, , .		5

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91	Practical proof of CP element based design for 14nm node and beyond. Proceedings of SPIE, 2013, , .	0.8	2
92	A structured routing architecture and its design methodology suitable for high-throughput electron beam direct writing with character projection. , 2013, , .		6
93	High-throughput electron beam direct writing of VIA layers by character projection using character sets based on one-dimensional VIA arrays with area-efficient stencil design. , 2013, , .		6
94	Session 26 overview: High-speed data converters. , 2013, , .		0
95	High-Throughput Electron Beam Direct Writing of VIA Layers by Character Projection with One-Dimensional VIA Characters. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 2458-2466.	0.3	1
96	CP element based design for 14nm node EBDW high volume manufacturing. Proceedings of SPIE, 2012, , .	0.8	12
97	All-Digital PMOS and NMOS Process Variability Monitor Utilizing Shared Buffer Ring and Ring Oscillator. IEICE Transactions on Electronics, 2012, E95.C, 627-634.	0.6	8
98	Frequency Resolution Enhancement for Digitally-Controlled Oscillator Based on a Single-Period Switching Scheme. IEICE Transactions on Electronics, 2012, E95.C, 1857-1863.	0.6	1
99	7.5Vmax arbitrary waveform generator with 65nm standard CMOS under 1.2V supply voltage. , 2012, , .		0
100	An integrated high-precision probe system for near-field magnetic measurements on cryptographic LSIs. , 2012, , .		5
101	Impact of All-Digital PLL on SoC Testing. , 2012, , .		1
102	A 580fs-Resolution Time-to-Digital Converter Utilizing Differential Pulse-Shrinking Buffer Ring in 0.18Âµm CMOS Technology. IEICE Transactions on Electronics, 2012, E95.C, 661-667.	0.6	5
103	An all-digital on-chip PMOS and NMOS process variability monitor utilizing shared buffer ring and ring oscillator. , 2011, , .		4
104	All-digital PMOS and NMOS process variability monitor utilizing buffer ring with pulse counter. , 2011, , .		2
105	A high frequency resolution Digitally-Controlled Oscillator using single-period switching scheme. , 2011, , .		4
106	All-digital ramp waveform generator for two-step single-slope ADC. IEICE Electronics Express, 2011, 8, 20-25.	0.8	2
107	All-Digital On-Chip Monitor for PMOS and NMOS Process Variability Utilizing Buffer Ring with Pulse Counter. IEICE Transactions on Electronics, 2011, E94-C, 487-494.	0.6	3
108	1.0 ps Resolution Time-to-Digital Converter Based-On Cascaded Time-Difference-Amplifier Utilizing Differential Logic Delay Cells. IEICE Transactions on Electronics, 2011, E94-C, 1098-1104.	0.6	2

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109	Cascaded Time Difference Amplifier with Differential Logic Delay Cell. IEICE Transactions on Electronics, 2011, E94-C, 654-662.	0.6	2
110	Time-to-digital converter based on time difference amplifier with non-linearity calibration. , 2010, , .		14
111	All-digital on-chip monitor for PMOS and NMOS process variability measurement utilizing buffer ring with pulse counter. , 2010, , .		17
112	A robust pulse delay circuit utilizing a differential buffer ring. , 2010, , .		10
113	An SoC platform with on-chip web interface for in-field monitoring. , 2009, , .		1
114	A fractionalâ€N MASH2â€k FDC phaseâ€locked loop architecture enabling higherâ€order quantisation noise shaping. Electronics Letters, 0, , .	1.0	0