Fawnizu Azmadi B Hussin

List of Publications by Year
in descending order

120 papers	764 citations	686830 13 h-index	713013 21 g-index
121 all docs	121 docs citations	121 times ranked	579 citing authors

#	Article	IF	Citations
1	Reliable Fault Tolerant-Based Multipath Routing Model for Industrial Wireless Control Systems. Applied Sciences (Switzerland), 2022, 12, 544.	1.3	20
2	An Arithmetic-Trigonometric Optimization Algorithm with Application for Control of Real-Time Pressure Process Plant. Sensors, 2022, 22, 617.	2.1	24
3	Application ofÂFractional-Order Signal Filtering Techniques forÂDead-Time Process Plants. Advances in Sustainability Science and Technology, 2022, , 811-824.	0.4	1
4	Optimal Coverage and Connectivity in Industrial Wireless Mesh Networks Based on Harrisâ€™ Hawk Optimization Algorithm. IEEE Access, 2022, 10, 51048-51061.	2.6	9
5	Carbon nanotube field effect transistor (<scp>CNTFET</scp>) operational transconductance amplifier (<scp>OTA</scp>) based design of high frequency memristor emulator. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2021, 34, e2827.	1.2	10
6	2-D Design of Double Gate Schottky Tunnel MOSFET for High-Performance Use in Analog/RF Applications. IEEE Access, 2021, 9, 80158-80169.	2.6	18
7	A Survey on the Application of WirelessHART for Industrial Process Monitoring and Control. Sensors, 2021, 21, 4951.	2.1	39
8	Design and Implementation of Signal Filtering Techniques on Real-time Pressure Process Plant. , 2021, , .		3
9	Carbon Nanotube Field Effect Transistor (CNTFET) and Resistive Random Access Memory (RRAM) Based Ternary Combinational Logic Circuits. Electronics (Switzerland), 2021, 10, 79.	1.8	41
10	Simulation and Control of Industrial Composition Process Over Wired and Wireless Networks. Lecture Notes on Data Engineering and Communications Technologies, 2021, , 685-695.	0.5	2
11	Ternary Arithmetic Logic Unit Design Utilizing Carbon Nanotube Field Effect Transistor (CNTFET) and Resistive Random Access Memory (RRAM). Micromachines, 2021, 12, 1288.	1.4	11
12	Energy-Efficient Superframe Scheduling in Industrial Wireless Networked Control System. Lecture Notes in Electrical Engineering, 2021, , 1227-1242.	0.3	1
13	Performance Analysis of CNTFET-ReRAM based Crossbar Network for In-Memory Computing. , 2021, , .		1
14	Design of Fractional-Order Predictive PI Controller for Real-time Pressure Process Plant. , 2021, , .		3
15	Fractional-Order Predictive PI Controller for Dead-Time Processes With Set-Point and Noise Filtering. IEEE Access, 2020, 8, 183759-183773.	2.6	25
16	FPGA-Based Lightweight Hardware Architecture of the PHOTON Hash Function for IoT Edge Devices. IEEE Access, 2020, 8, 207610-207618.	2.6	12
17	Fractional-order Predictive PI Controller for Process Plants with Deadtime. , 2020, , .		5
18	Simulation and Control of Inverted Pendulum System Dynamics over Control Area Network using TrueTime. , 2020, , .		2

#	Article	IF	Citations
19	Single event burnout hardening of trench shielded power UMOSFET using High-Î¹ dielectrics. Materials Research Express, 2020, 7, 035907.	0.8	1
20	Bio-Inspired Solutions and Its Impact on Real-World Problems: A Network on Chip (NoC) Perspective. , 2019, , .		0
21	Bleeding detection in wireless capsule endoscopy videos â€" Color versus texture features. Journal of Applied Clinical Medical Physics, 2019, 20, 141-154.	0.8	32
22	An Efficient Implementation of LED Block Cipher on FPGA. , 2019, , .		7
23	Machine-Learning-Based Multiple Abstraction-Level Detection of Hardware Trojan Inserted at Register-Transfer Level. , 2019, , .		3
24	Enhanced Trench Shielded Power UMOSFET for Single Event Burnout Hardening. , 2019, , .		7
25	IoT Based Vehicle Emission Monitoring and Alerting System. , 2019, , .		14
26	Net Classification Based on Testability and Netlist Structural Features for Hardware Trojan Detection. , 2019, , .		15
27	Bio-inspired network on chip having both guaranteed throughput and best effort services using fault-tolerant algorithm. IEEJ Transactions on Electrical and Electronic Engineering, 2018, 13, 1153-1162.	0.8	1
28	Fine-Grained Overhead Analysis Utilizing Atomic Instructions for Cross-ISA Dynamic Binary Translation on Multicore Processor. , 2018, , .		0
29	Fine-Grained Overhead Characterisation of Cross-ISA DBTO for Multicore Processor. Indonesian Journal of Electrical Engineering and Computer Science, 2018, 10, 1036.	0.7	0
30	Bio-inspired fault tolerant network on chip. The Integration VLSI Journal, 2017, 58, 155-166.	1.3	4
31	Localization of optic disc and fovea in retinal images using intensity based line scanning analysis. Computers in Biology and Medicine, 2017, 87, 382-396.	3.9	35
32	Detection and Classification of Bleeding Region in WCE Images using Color Feature. , 2017, , .		20
33	Offline Error Detection in MEDA-Based Digital Microfluidic Biochips Using Oscillation-Based Testing Methodology. Journal of Electronic Testing: Theory and Applications (JETTA), 2017, 33, 621-635.	0.9	10
34	A Hybrid Delay Design-for-Testability for Nonseparable RTL Controller-Data Path Circuits. Journal of Circuits, Systems and Computers, 2017, 26, 1750021.	1.0	0
35	Minimizing scheduling overhead in LRE-TL real-time multiprocessor scheduling algorithm. Turkish Journal of Electrical Engineering and Computer Sciences, 2017, 25, 263-277.	0.9	0
36	Advances in Testing Techniques for Digital Microfluidic Biochips. Sensors, 2017, 17, 1719.	2.1	16

#	Article	IF	Citations
37	Feature Selection and Classification of Ulcerated Lesions Using Statistical Analysis for WCE Images. Applied Sciences (Switzerland), 2017, 7, 1097.	1.3	26
38	Review of Network on Chip Architectures. Recent Advances in Electrical and Electronic Engineering, 2017, 10, .	0.2	1
39	Implementation and Analysis of Biological Synaptogenesis Technique on Nodes and Interconnects for NoC Fault Tolerance. Research Journal of Applied Sciences, Engineering and Technology, 2016, 12, 483-489.	0.1	2
40	Detection and classification of bleeding using statistical color features for wireless capsule endoscopy images. , 2016, , .		5
41	False path identification algorithm framework for nonseparable controller-data path circuits. , 2016, , .		0
42	Biologically inspired network on chip fault tolerant algorithm using time division multiplexing. , 2016, , .		1
43	Dual-Engine Cross-ISA DBTO Technique Utilising MultiThreaded Support for Multicore Processor System. , 2016, , .		2
44	Automatic detection and removal of bubble frames from wireless capsule endoscopy video sequences. , 2016, , .		2
45	Investigation of capacitance dependence on droplet volume in MEDA based biochips. , 2016, , .		4
46	Fault Modeling and Simulation of MEDA Based Digital Microfluidics Biochips. , 2016, , .		6
47	Bio-inspired NoC fault tolerant techniques using guaranteed throughput and best effort services. The Integration VLSI Journal, 2016, 54, 65-96.	1.3	4
48	Ulcer Detection and Classification of Wireless Capsule Endoscopy Images Using RGB Masking. Advanced Science Letters, 2016, 22, 2764-2768.	0.2	7
49	Review of Single Cycle Shifter for Structured LDPC Encoder. Applied Mechanics and Materials, 2015, 763, 189-194.	0.2	0
50	On enhancing the reliability of digital microfluidic biochips (DMFB) through electrode cells health classification. , 2015, , .		3
51	Delay design-for-testability for functional RTL circuits. , 2015, , .		0
52	An Energy Efficient Cross-Layer Network Operation Model for IEEE 802.15.4-Based Mobile Wireless Sensor Networks. IEEE Sensors Journal, 2015, 15, 684-692.	2.4	68
53	Resistive Open Faults Detectability Analysis and Implications for Testing Low Power Nanometric ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 580-583.	2.1	1
54	Optimum Colour Space Selection for Ulcerated Regions Using Statistical Analysis and Classification of Ulcerated Frames from WCE Video Footage. Lecture Notes in Computer Science, 2015, , 373-381.	1.0	3

#	Article	IF	Citations
55	On Location Estimation Methods for Mobile Wireless Sensor Nodes. Research Journal of Applied Sciences, Engineering and Technology, 2014, 8, 124-130.	0.1	0
56	Enhancement in IEEE 1500 standard for at-speed test and debug. , 2014, , .		0
57	Automated train track misalignment detection system based on inertia measurement unit. , 2014, , .		1
58	A semi greedy soft real-time multiprocessor scheduling algorithm. , 2014, , .		2
59	Multivoltage Aware Resistive Open Fault Model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 220-231.	2.1	1
60	Automatic generation of test instructions for path delay faults based-on stuck-at fault in processor cores using assignment decision diagram. , 2014, , .		3
61	Diagonal testing in digital microfluidics biochips using MEDA based approach. , 2014, , .		5
62	Enhancement in IEEE 1500 standard for at-speed functional testing. , 2014, , .		0
63	Bio-inspired NoC fault tolerant techniques. , 2014, , .		3
64	Optimized encoder architecture for structured low density parity check codes of short length. , 2014, , .		2
65	Image Enhancement Using Geometric Mean Filter and Gamma Correction for WCE Images. Lecture Notes in Computer Science, 2014, , 276-283.	1.0	14
66	Acceleration of Retinex Algorithm for Image Processing on Android Device Using Renderscript. Lecture Notes in Electrical Engineering, 2014, , 137-143.	0.3	1
67	Reducing Tasks Migration in LRE-TL Real-time Multiprocessor Scheduling Algorithm. Procedia Technology, 2013, 11, 235-242.	1.1	1
68	Survey and Evaluation of Automated Model Generation Techniques for High Level Modeling and High Level Fault Modeling. Journal of Electronic Testing: Theory and Applications (JETTA), 2013, 29, 861-877.	0.9	4
69	Synaptogenesis based bio-inspired NoC fault tolerant interconnects. , 2013, , .		6
70	SEOS: Hardware Implementation of Real-Time Operating System for Adaptability. , 2013, , .		28
71	A wide-range programmable frequency synthesizer based on a finite state machine filter. International Journal of Electronics, 2013, 100, 1546-1556.	0.9	0
72	On using IEEE 1500 standard for functional testing. , 2013, , .		0

#	Article	IF	Citations
73	Automatic generation of test instructions for structural faults in processor cores using satisfiability. , 2013, , .		3
74	Optimization of blood vessel detection in retina images using multithreading and native code for portable devices. , 2013, , .		1
75	On testing of MEDA based digital microfluidics biochips. , 2013, , .		13
76	Implementation of biological sprouting algorithm for NoC fault tolerance. , 2013, , .		6
77	Automated Model Generation of Analog Circuits through Modified Trajectory Piecewise Linear Approach with Cheby Shev Newton Interpolating Polynomials. , 2013, , .		1
78	High throughput architecture for low density parity check (LDPC) encoder. , 2013, , .		1
79	A Novel Algorithm for Automated Model Generation of Analog Circuits Using Chebyshev-Newton Interpolation. Advanced Science Letters, 2013, 19, 1520-1524.	0.2	0
80	Fault Modeling of Analog Circuits Using System Identification Automated Model Generation Approaches from SPICE Level Descriptions. Advanced Science Letters, 2013, 19, 1276-1280.	0.2	0
81	A review of TiO[sub 2] nanotube arrays for hydrogen sensing application. , 2012, , .		2
82	Design for cold test elimination - facing the Inverse Temperature Dependence (ITD) challenge. , 2012, , .		0
83	An energy efficient localization estimation approach for mobile wireless sensor networks. , 2012, , .		3
84	A review of the current status of the Java programming on embedded real-time systems. , 2012, , .		0
85	Pipelined architecture for low density parity check encoder. , 2012, , .		0
86	High level fault modeling and fault propagation in analog circuits using NLARX automated model generation technique. , 2012, , .		7
87	FPGA-based hardware implementation of optical flow constraint equation of Horn and Schunck. , 2012, , .		7
88	Modular body sensor system design for plug-and-play monitoring system. , 2012, , .		0
89	Resistance dependent delay behaviour of resistive open faults in multi voltage designs. , 2012, , .		0
90	Multi-voltage aware resistive open fault modeling. , 2012, , .		1

#	Article	IF	Citations
91	A link-quality and energy aware routing metric for mobile wireless sensor networks. , 2012, , .		3
92	Design and FPGA implementation of PLL-based quarter-rate clock and data recovery circuit. , 2012, , .		2
93	An optimal design of moving objects tracking algorithm on FPGA. , 2012, , .		1
94	Detectability analysis for resistive open faults with dynamic supply voltage scaling awareness. , 2011, , .		3
95	Propagation of delay faults caused by resistive open faults with dynamic voltage scaling awareness. , 2011, , .		1
96	High rate (3, k) regular LDPC encoder architecture. , 2011, , .		0
97	Road sign detection and recognition system for real-time embedded applications. , 2011, , .		18
98	A case study of process-variation effect to SoC analog circuits. , 2011, , .		1
99	Hardware architecture of OFCE-HS for hardware implementation. Proceedings of SPIE, 2011, , .	0.8	1
100	NBTI-induced 8-Bit DAC circuit mismatch in System-On-Chip (SoC). , 2011, , .		2
101	Development of TiO<inf>2</inf> nanotubes for hydrogen sensing application. , 2011, , .		0
102	A gradient coprocessor of optical flow: A hardware co-simulation using FPGA based on MAC-DA. , 2011, , .		0
103	IDVP (Intra-Die Variation Probe) for System-On-Chip (SoC) Infant Mortality screen. , 2011, , .		1
104	Investigation of Collaborative Interaction Using ITB-Based Setting vs. Computer-Based Setting. Communications in Computer and Information Science, 2011, , 354-368.	0.4	1
105	Hardware implementation of an optimized processor architecture for SOBEL image edge detection operator. , 2010, , .		9
106	A case study for reliability-aware in SoC analog circuit design. , 2010, , .		0
107	Camera Sensor network localization using FPGA. , 2010, , .		0
108	Optimization of Processor Architecture for Image Edge Detection Filter. , 2010, , .		10

#	Article	IF	Citations
109	Space Vector PWM for PMSM simulation using Matlab Simulink. , 2010, , .		6
110	Shape-based road sign detection and recognition for embedded application using MATLAB. , 2010, , .		6
111	RedSOCs-3D: Thermal-safe test scheduling for 3D-stacked SOC. , 2010, , .		6
112	Serpent encryption algorithm implementation on Compute Unified Device Architecture (CUDA). , 2009, , .		7
113	NoC-Compatible Wrapper Design and Optimization under Channel-Bandwidth and Test-Time Constraints. IEICE Transactions on Information and Systems, 2008, E91-D, 2008-2017.	0.4	4
114	On NoC Bandwidth Sharing for the Optimization of Area Cost and Test Application Time. IEICE Transactions on Information and Systems, 2008, E91-D, 1999-2007.	0.4	1
115	Scheduling Power-Constrained Tests through the SoC Functional Bus. IEICE Transactions on Information and Systems, 2008, E91-D, 736-746.	0.4	0
116	Area Overhead and Test Time Co-Optimization through NoC Bandwidth Sharing. , 2007, , .		1
117	Core-Based Testing of Multiprocessor System-on-Chips Utilizing Hierarchical Functional Buses. , 2007, , .		5
118	Optimization of NoC Wrapper Design under Bandwidth and Test Time Constraints. Proceedings of the IEEE European Test Workshop, 2007, , .	0.0	23
119	Area Overhead and Test Time Co-Optimization through NoC Bandwidth Sharing. Proceedings of the Asian Test Symposium, 2007, , .	0.0	0
120	Power-Constrained SOC Test Schedules through Utilization of Functional Buses. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	9