Pramod Kumar Tiwari

List of Publications by Year
in descending order

53	493	759233 12	752698 20
papers	citations	h-index	g-index

53	53	53	280
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Self-heating and Negative Differential Conductance Improvement by Substrate Bias Voltage in Tri-gate Junctionless Transistor. Silicon, 2022, 14, 2219-2224.	3.3	1
2	Investigating the Impact of Self-Heating Effects on some Thermal and Electrical Characteristics of Dielectric Pocket Gate-all-around (DPGAA) MOSFETs. Silicon, 2022, 14, 7053-7063.	3.3	7
3	Physical Insight into Self-heating Induced Performance Degradation in RingFET. Silicon, 2022, 14, 7585-7593.	3.3	2
4	Impact of Self-Heating on Linearity Performance of In_{0.53}Ga_{0.47}As-Based Gate-All-Around MOSFETs. IEEE Transactions on Device and Materials Reliability, 2022, 22, 42-49.	2.0	4
5	Sensitivity Analysis of Silicon Nanotube FET (Si NTFET) with TCAD Assisted Machine Learning. Silicon, 2022, 14, 9021-9031.	3.3	4
6	Subthreshold Modeling of GAA MOSFET Including the Effect of Process-Induced Inclined Sidewalls. IEEE Transactions on Electron Devices, 2022, 69, 487-494.	3.0	6
7	Split-Gate Induced High-Field for Impact Ionization Triggered Bipolar Action and Sub-kT/q Switching in Junctionless FET. IEEE Nanotechnology Magazine, 2022, 21, 332-339.	2.0	0
8	Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs. Silicon, 2021, 13, 1231-1238.	3.3	8
9	Threshold Voltage Modeling of tri-Gate Schottky-Barrier (TGSB) Field-Effect-Transistors (FETs). Silicon, 2021, 13, 25-35.	3.3	0
10	Thermal Noise Models for Trigate Junctionless Transistors Including Substrate Bias Effects. IEEE Transactions on Electron Devices, 2020, 67, 263-269.	3.0	6
11	Investigating linearity and effect of temperature variation on analog/RF performance of dielectric pocket high-k double gate-all-around (DP-DGAA) MOSFETs. Applied Physics A: Materials Science and Processing, 2020, 126, 1.	2.3	9
12	Investigation of Temperature and Source/Drain Overlap Impact on Negative Capacitance Silicon Nanotube FET (NC Si NTFET) with Sub-60mV/decade Switching. IEEE Nanotechnology Magazine, 2020, 19, 800-806.	2.0	7
13	Investigation of Ring-TFET for Better Electrostatics Control and Suppressed Ambipolarity. IEEE Nanotechnology Magazine, 2020, 19, 829-836.	2.0	7
14	Simulation Study of Dielectric Modulated Dual Channel Trench Gate TFET-Based Biosensor. IEEE Sensors Journal, 2020, 20, 12565-12573.	4.7	46
15	Self-heating effects and hot carrier degradation in In_{0.53}Ga_{0.47}As gate-all-around MOSFETs. Semiconductor Science and Technology, 2020, 35, 065008.	2.0	10
16	Physical Insight into Self-heating Effects in Ultrathin Junctionless Gate-All-Around FETs. , 2019, , .		5
17	An Insight Into Self-Heating Effects and Its Implications on Hot Carrier Degradation for Silicon-Nanotube-Based Double Gate-All-Around (DGAA) MOSFETs. IEEE Journal of the Electron Devices Society, 2019, 7, 1100-1108.	2.1	11
18	Static and Quasi-Static Drain Current Modeling of Tri-Gate Junctionless Transistor With Substrate Bias-Induced Effects. IEEE Transactions on Electron Devices, 2019, 66, 2876-2883.	3.0	17

#	Article	IF	Citations
19	A Proposal for an Electrostatic Doping-Assisted Electroabsorption Modulator for Intrachip Communication. IEEE Transactions on Electron Devices, 2019, 66, 2269-2275.	3.0	8
20	Subthreshold Characteristic Analysis and Models for Tri-Gate SOI MOSFETs Using Substrate Bias Induced Effects. IEEE Nanotechnology Magazine, 2019, 18, 329-335.	2.0	15
21	Temperature Dependence of Subthreshold Characteristics of Negative Capacitance Recessed-Source/Drain (NC R-S/D) SOI MOSFET. , 2019, , .		2
22	Drain current modelling of double gateâ€allâ€around (DGAA) MOSFETs. IET Circuits, Devices and Systems, 2019, 13, 519-525.	1.4	10
23	Analytical Modeling of Subthreshold Current and Subthreshold Swing of Schottky-Barrier Source/Drain Double Gate-All-Around (DGAA) MOSFETs. , 2019, , .		0
24	Modeling of Drain Current and Analog Characteristics of Dual-Metal Quadruple Gate (DMQG) MOSFETs. , 2019, , .		0
25	Investigation of Thermal Noise in Trigate Junctionless Transistor. , 2019, , .		0
26	Analytical Modeling of Analog/RF Parameters for Trigate Junctionless Field Effect Transistor Incorporating Substrate Biasing Effects. , 2019, , .		1
27	Compact Drain Current Model of Silicon-Nanotubebased Double Gate-All-Around (DGAA) MOSFETs Incorporating Short Channel Effects. , 2019, , .		3
28	Subthreshold Modeling of Tri-Gate Junctionless Transistors With Variable Channel Edges and Substrate Bias Effects. IEEE Transactions on Electron Devices, 2018, 65, 1663-1671.	3.0	29
29	An Explicit Unified Drain Current Model for Silicon-Nanotube-Based Ultrathin Double Gate-All-Around <sc> mosfet</sc>s. IEEE Nanotechnology Magazine, 2018, 17, 1224-1234.	2.0	11
30	Analytical Subthreshold Current and Subthreshold Swing Models for a Fully Depleted (FD) Recessed-Source/Drain (Re-S/D) SOI MOSFET with Back-Gate Control. Journal of Electronic Materials, 2017, 46, 5046-5056.	2.2	0
31	Analytical modeling of subthreshold characteristics of ultra-thin double gate-all-around (DGAA) MOSFETs incorporating quantum confinement effects. Superlattices and Microstructures, 2017, 109, 567-578.	3.1	17
32	Ferro-electric stacked gate oxide heterojunction electro-statically doped source/drain double-gate tunnel field effect transistors: A superior structure. Materials Science in Semiconductor Processing, 2017, 71, 161-165.	4.0	20
33	Theoretical and Experimental Study of UV Detection Characteristics of Pd/ZnO Nanorod Schottky Diodes. Nano, 2017, 12, 1750137.	1.0	4
34	A Threshold Voltage Model of Silicon-Nanotube-Based Ultrathin Double Gate-All-Around (DGAA) MOSFETs Incorporating Quantum Confinement Effects. IEEE Nanotechnology Magazine, 2017, 16, 868-875.	2.0	40
35	A Threshold Voltage Model of Tri-Gate Junctionless Field-Effect Transistors Including Substrate Bias Effects. IEEE Transactions on Electron Devices, 2017, 64, 3534-3540.	3.0	24
36	An analytical subthreshold current model of short-channel symmetrical double gate-all-around (DGAA) field-effect-transistors. , 2017, , .		3

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37	An Analytical Threshold Voltage Model of Fully Depleted (FD) Recessed-Source/Drain (Re-S/D) SOI MOSFETs with Back-Gate Control. Journal of Electronic Materials, 2016, 45, 5367-5374.	2.2	3
38	Threshold voltage modeling for dualâ€metal quadrupleâ€gate (DMQG) MOSFETs. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2016, 29, 695-706.	1.9	4
39	Analytical modeling of threshold voltage for symmetrical silicon nano-tube field-effect-transistors (Si-NT FETs). Journal of Computational Electronics, 2016, 15, 516-524.	2.5	25
40	Quasi-3D subthreshold current and subthreshold swing models of dual-metal quadruple-gate (DMQG) MOSFETs. Journal of Computational Electronics, 2015, 14, 582-592.	2.5	11
41	A performance analysis of Hetero- Dielectric Dual-Material-Gate silicon-on-insulator tunnel field effect transistors (HD-DMG SOI TFETs). , 2014, , .		3
42	A Two-Dimensional Subthreshold Current Model of Recessed-Source/Drain (Re-S/D) SOI MOSFETs with High-k Dielectric. , 2014, , .		1
43	ATLAS™ based simulation study of the electrical characteristics of dual-metal-gate (DMG) fully-depleted (FD) recessed-source/drain (Re-S/D) SOI MOSFETs. , 2014, , .		1
44	Analytical subthreshold current and subthreshold swing models of short-channel dual-metal-gate (DMG) fully-depleted recessed-source/drain (Re-S/D) SOI MOSFETs. Journal of Computational Electronics, 2014, 13, 467-476.	2.5	6
45	A threshold voltage model of short-channel fully-depleted recessed-source/drain (Re-S/D) UTB SOI MOSFETs including substrate induced surface potential effects. Solid-State Electronics, 2014, 95, 52-60.	1.4	19
46	Two-dimensional modeling of subthreshold current and subthreshold swing of double-material-gate (DMG) strained-Si (s-Si) on SGOI MOSFETs. Journal of Computational Electronics, 2013, 12, 275-280.	2.5	9
47	An analytical model of threshold voltage for short-channel double-material-gate (DMG) strained-Si (s-Si) on Silicon-Germanium-on-Insulator (SGOI) MOSFETs. Journal of Computational Electronics, 2013, 12, 20-28.	2.5	23
48	An Analytical Threshold Voltage Model for Triple-Material Cylindrical Gate-All-Around (TM-CGAA) MOSFETs. IEEE Nanotechnology Magazine, 2013, 12, 766-774.	2.0	46
49	An analytical modeling of interface charge induced effects on subthreshold current and subthreshold swing of strained-Si (s-Si) on Silicon-Germinium-on-Insulator (SGOI) MOSFETs. , 2012, , .		0
50	A 2D analytical modeling approach for nanoscale strained-Si (s-Si) on silicon-germanium-on-insulator (SGOI) MOSFETs by evanescent mode analysis. , 2012, , .		0
51	Analytical modeling and ATLAS™ based simulation of the surface potential of double-material-gate strained-Si on Silicon-Germanium-on-Insulator (DMGSGOI) MOSFETs. , 2011, , .		1
52	Effect of Self-Heating on Small-Signal Parameters of In0.53Ga0.47As Based Gate-All-Around MOSFETs. Semiconductor Science and Technology, 0, , .	2.0	0
53	Exploring the Self-Heating Effects & Its Impact on Thermal Noise for Dielectric Pocket Packed Double-Gate-All-Around (DPP-DGAA) MOSFETs. Silicon, 0, , 1.	3.3	4