Tsu-Jae Liu

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

124 papers	3,370 citations	26 h-index	55 g-index
139 ext. papers	4,077 ext. citations	3.1 avg, IF	5.24 L-index

#	Paper	IF	Citations
124	Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec. *IEEE Electron Device Letters*, **2007**, 28, 743-745	4.4	1160
123	Demonstration of L-Shaped Tunnel Field-Effect Transistors. *IEEE Transactions on Electron Devices*, **2016**, 63, 1774-1778	2.9	161
122	Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off. *IEEE Journal of Solid-State Circuits*, **2008**, 43, 600-609	5.5	131
121	Tunnel Field Effect Transistor With Raised Germanium Source. *IEEE Electron Device Letters*, **2010**, 31, 1107-1109	4.4	113
120	Large-Scale SRAM Variability Characterization in 45 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 3174-3192	5.5	94
119	Study of Random Dopant Fluctuation Induced Variability in the Raised-Ge-Source TFET. *IEEE Electron Device Letters*, **2013**, 34, 184-186	4.4	92
118	Gate Line Edge Roughness Model for Estimation of FinFET Performance Variability. *IEEE Transactions on Electron Devices*, **2009**, 56, 3055-3063	2.9	70
117	Study of Random-Dopant-Fluctuation (RDF) Effects for the Trigate Bulk MOSFET. *IEEE Transactions on Electron Devices*, **2009**, 56, 1538-1542	2.9	66
116	Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages **2008**,		55
115	A Comparative Study of Dopant-Segregated Schottky and Raised Source/Drain Double-Gate MOSFETs. *IEEE Transactions on Electron Devices*, **2008**, 55, 2665-2677	2.9	50
114	Prospect of tunneling green transistor for 0.1V CMOS **2010**,		47
113	Tri-Gate Bulk MOSFET Design for CMOS Scaling to the End of the Roadmap. *IEEE Electron Device Letters*, **2008**, 29, 491-493	4.4	45
112	SRAM Read/Write Margin Enhancements Using FinFETs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 887-900	2.6	44
111	Characterization of Dynamic SRAM Stability in 45 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 2702-2712	5.5	42
110	Nano-Electro-Mechanical Nonvolatile Memory (NEMory) Cell Design and Scaling. *IEEE Transactions on Electron Devices*, **2008**, 55, 3482-3488	2.9	41
109	Mechanically modulated tunneling resistance in monolayer MoS2. *Applied Physics Letters*, **2013**, 103, 183105	3.4	36
108	Perfectly Complementary Relay Design for Digital Logic Applications. *IEEE Electron Device Letters*, **2010**, 31, 371-373	4.4	36

107	Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes. *Journal of Microelectromechanical Systems*, **2012**, 21, 511-513	2.5	36
106	Dopant-Segregated Schottky Source/Drain Double-Gate MOSFET Design in the Direct Source-to-Drain Tunneling Regime. *IEEE Transactions on Electron Devices*, **2009**, 56, 2016-2026	2.9	34
105	Effectiveness of Stressors in Aggressively Scaled FinFETs. *IEEE Transactions on Electron Devices*, **2012**, 59, 1592-1598	2.9	33
104	FinFET Evolution Toward Stacked-Nanowire FET for CMOS Technology Scaling. *IEEE Transactions on Electron Devices*, **2015**, 62, 3945-3950	2.9	31
103	Performance and Area Scaling Benefits of FD-SOI Technology for 6-T SRAM Cells at the 22-nm Node. *IEEE Transactions on Electron Devices*, **2010**, 57, 1301-1309	2.9	30
102	Germanium Gate PhotoMOSFET Integrated to Silicon Photonics. *IEEE Journal of Selected Topics in Quantum Electronics*, **2014**, 20, 1-7	3.8	29
101	Compact Nano-Electro-Mechanical Non-Volatile Memory (NEMory) for 3D Integration **2007**,		29
100	Design Optimization of Multigate Bulk MOSFETs. *IEEE Transactions on Electron Devices*, **2013**, 60, 28-33	2.9	27
99	Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions. *Journal of Microelectromechanical Systems*, **2014**, 23, 198-203	2.5	27
98	Hybrid CMOS/BEOL-NEMS technology for ultra-low-power IC applications **2014**,		26
97	MOSFET design for forward body biasing scheme. *IEEE Electron Device Letters*, **2006**, 27, 387-389	4.4	26
96	Seesaw Relay Logic and Memory Circuits. *Journal of Microelectromechanical Systems*, **2010**, 19, 1012-1014	2.5	25
95	Impact of Body Doping and Thickness on the Performance of Germanium-Source TFETs. *IEEE Transactions on Electron Devices*, **2010**, 57, 1710-1713	2.9	25
94	ZrO2 Ferroelectric FET for Non-volatile Memory Application. *IEEE Electron Device Letters*, **2019**, 40, 1419-1422	4.4	24
93	Characterization of Polycrystalline Silicon-Germanium Film Deposition for Modularly Integrated MEMS Applications. *Journal of Microelectromechanical Systems*, **2007**, 16, 68-77	2.5	21
92	Four-Terminal-Relay Body-Biasing Schemes for Complementary Logic Circuits. *IEEE Electron Device Letters*, **2010**, 31, 890-892	4.4	18
91	Carrier-Mobility Enhancement via Strain Engineering in Future Thin-Body MOSFETs. *IEEE Electron Device Letters*, **2012**, 33, 318-320	4.4	17
90	Design Requirements for Steeply Switching Logic Devices. *IEEE Transactions on Electron Devices*, **2012**, 59, 326-334	2.9	17

89	Spacer Gate Lithography for Reduced Variability Due to Line Edge Roughness. *IEEE Transactions on Semiconductor Manufacturing*, **2010**, 23, 311-315	2.6	17
88	Scaling Limitations for Flexural Beams Used in Electromechanical Devices. *IEEE Transactions on Electron Devices*, **2009**, 56, 688-691	2.9	16
87	Three-Dimensional FinFET Source/Drain and Contact Design Optimization Study. *IEEE Transactions on Electron Devices*, **2009**, 56, 1483-1492	2.9	16
86	Dopant-Segregated Schottky Junction Tuning With Fluorine Pre-Silicidation Ion Implant. *IEEE Transactions on Electron Devices*, **2010**, 57, 1084-1092	2.9	15
85	Planar GeOI TFET Performance Improvement With Back Biasing. *IEEE Transactions on Electron Devices*, **2012**, 59, 1629-1635	2.9	14
84	Comparative Study of Uniform Versus Supersteep Retrograde MOSFET Channel Doping and Implications for 6-T SRAM Yield. *IEEE Transactions on Electron Devices*, **2013**, 60, 1790-1793	2.9	14
83	Simulation-Based Study of Hybrid Fin/Planar LDMOS Design for FinFET-Based System-on-Chip Technology. *IEEE Transactions on Electron Devices*, **2017**, 64, 4193-4199	2.9	14
82	Simulation-Based Study of the Inserted-Oxide FinFET for Future Low-Power System-on-Chip Applications. *IEEE Electron Device Letters*, **2015**, 36, 742-744	4.4	14
81	Nanomechanical Switch Designs to Overcome the Surface Adhesion Energy Limit. *IEEE Electron Device Letters*, **2015**, 36, 963-965	4.4	14
80	Four-Terminal Relay Design for Improved Body Effect. *IEEE Electron Device Letters*, **2010**, 31, 515-517	4.4	14
79	Non-Volatile Nano-Electro-Mechanical Memory for Energy-Efficient Data Searching. *IEEE Electron Device Letters*, **2016**, 37, 31-34	4.4	13
78	Effect of Body Biasing on the Energy-Delay Performance of Logic Relays. *IEEE Electron Device Letters*, **2015**, 36, 862-864	4.4	13
77	Variation-Aware Comparative Study of 10-nm GAA Versus FinFET 6-T SRAM Performance and Yield. *IEEE Transactions on Electron Devices*, **2014**, 61, 3949-3954	2.9	13
76	A 1.2V, 2.4GHz Fully Integrated Linear CMOS Power Amplifier with Efficiency Enhancement **2006**,		13
75	High-Mobility Ge pMOSFETs With Crystalline ZrO2 Dielectric. *IEEE Electron Device Letters*, **2019**, 40, 371-374	4.4	12
74	Design of Gate-All-Around Silicon MOSFETs for 6-T SRAM Area Efficiency and Yield. *IEEE Transactions on Electron Devices*, **2014**, 61, 2371-2377	2.9	12
73	Electromechanical Diode Cell for Cross-Point Nonvolatile Memory Arrays. *IEEE Electron Device Letters*, **2012**, 33, 131-133	4.4	12
72	Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits. *IEEE Electron Device Letters*, **2012**, 33, 281-283	4.4	12

71	Pull-In and Release Voltage Design for Nanoelectromechanical Field-Effect Transistors. *IEEE Transactions on Electron Devices*, **2009**, 56, 3072-3082	2.9	12
70	MOSFET hot-carrier reliability improvement by forward-body bias. *IEEE Electron Device Letters*, **2006**, 27, 605-608	4.4	12
69	Impact of back biasing on carrier transport in ultra-thin-body and BOX (UTBB) Fully Depleted SOI MOSFETs **2012**,		11
68	Physically Based Modeling of Stress-Induced Variation in Nanoscale Transistor Performance. *IEEE Transactions on Device and Materials Reliability*, **2011**, 11, 378-386	1.6	11
67	Channel Stress and Ballistic Performance Advantages of Gate-All-Around FETs and Inserted-Oxide FinFETs. *IEEE Nanotechnology Magazine*, **2017**, 16, 209-216	2.6	10
66	Impact of Gate Line-Edge Roughness (LER) Versus Random Dopant Fluctuations (RDF) on Germanium-Source Tunnel FET Performance. *IEEE Nanotechnology Magazine*, **2013**, 12, 1061-1067	2.6	10
65	Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage **2012**,		10
64	The Effect of Random Dopant Fluctuation on Specific Contact Resistivity. *IEEE Transactions on Electron Devices*, **2010**, 57, 273-281	2.9	10
63	A Novel Self-Aligned 4-Bit SONOS-Type Nonvolatile Memory Cell With T-Gate and I-Shaped FinFET Structure. *IEEE Transactions on Electron Devices*, **2010**, 57, 1728-1736	2.9	10
62	Nanocrystal-Embedded-Insulator Ferroelectric Negative Capacitance FETs With Sub-kT/q Swing. *IEEE Electron Device Letters*, **2018**, 1-1	4.4	10
61	Embedded Nano-Electro-Mechanical Memory for Energy-Efficient Reconfigurable Logic. *IEEE Electron Device Letters*, **2016**, 37, 1563-1565	4.4	9
60	Extension of Planar Bulk n-Channel MOSFET Scaling With Oxygen Insertion Technology. *IEEE Transactions on Electron Devices*, **2014**, 61, 3345-3349	2.9	9
59	Interfacial Adhesion between Rough Surfaces of Polycrystalline Silicon and Its Implications for M/NEMS Technology. *Journal of Adhesion Science and Technology*, **2010**, 24, 2545-2556	2	9
58	Scale-Length Assessment of the Trigate Bulk MOSFET Design. *IEEE Transactions on Electron Devices*, **2009**, 56, 2840-2842	2.9	9
57	Flicker-Noise Impact on Scaling of Mixed-Signal CMOS With HfSiON. *IEEE Transactions on Electron Devices*, **2008**, 55, 417-422	2.9	9
56	Impact of Gate-Induced Strain on MuGFET Reliability. *IEEE Electron Device Letters*, **2008**, 29, 916-919	4.4	9
55	Prospects for MEM logic switch technology **2010**,		8
54	DSS MOSFET With Tunable SDE Regions by Fluorine Pre-Silicidation Ion Implant. *IEEE Electron Device Letters*, **2010**, 31, 785-787	4.4	8

53	Enhanced endurance of dual-bit SONOS NVM cells using the GIDL read method **2008**,		8
52	Compensation of systematic variations through optimal biasing of SRAM wordlines **2008**,		8
51	Energy-delay performance optimization of NEM logic relay **2015**,		7
50	Large-scale read/write margin measurement in 45nm CMOS SRAM arrays **2008**,		7
49	Variability Study for Low-Voltage Microelectromechanical Relay Operation. *IEEE Transactions on Electron Devices*, **2018**, 65, 1529-1534	2.9	6
48	Microelectromechanical Relay and Logic Circuit Design for Zero Crowbar Current. *IEEE Transactions on Electron Devices*, **2014**, 61, 3296-3302	2.9	6
47	NEM relay design for compact, ultra-low-power digital logic circuits **2014**,		6
46	MOSFET performance and scalability enhancement by insertion of oxygen layers **2012**,		6
45	Study of High-Performance Ge pMOSFET Scaling Accounting for Direct Source-to-Drain Tunneling. *IEEE Transactions on Electron Devices*, **2011**, 58, 2895-2902	2.9	6
44	Convex Channel Design for Improved Capacitorless DRAM Retention Time **2009**,		6
43	Reliability of Nanoelectromechanical Nonvolatile Memory (NEMory) Cells. *IEEE Electron Device Letters*, **2009**, 30, 269-271	4.4	6
42	FinFET Design for Tolerance to Statistical Dopant Fluctuations. *IEEE Nanotechnology Magazine*, **2009**, 8, 375-378	2.6	6
41	Demonstration of 50-mV Digital Integrated Circuits with Microelectromechanical Relays **2018**,		6
40	Threshold Voltage and DIBL Variability Modeling Based on Forward and Reverse Measurements for SRAM and Analog MOSFETs. *IEEE Transactions on Electron Devices*, **2015**, 62, 1119-1126	2.9	5
39	Tilted ion implantation as a cost-efficient sublithographic patterning technique. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2016**, 34, 040608	1.3	5
38	Recent progress and challenges for relay logic switch technology **2012**,		5
37	Fabrication of $hbox{Si}_{1 - x}hbox{Ge}_{x}/hbox{Si}$ pMOSFETs Using Corrugated Substrates for Improved $I_{rm ON}$ and Reduced Layout-Width Dependence. *IEEE Transactions on Electron Devices*, **2013**, 60, 153-158	2.9	5
36	Dual-Bit Gate-Sidewall Storage FinFET NVM and New Method of Charge Detection. *IEEE Electron Device Letters*, **2007**, 28, 502-505	4.4	5

35	Reducing adhesion energy of nano-electro-mechanical relay contacts by self-assembled Perfluoro (2,3-Dimethylbutan-2-ol) coating. *AIP Advances*, **2019**, 9, 055329	1.5	4
34	Effects of oxygen-inserted layers on diffusion of boron, phosphorus, and arsenic in silicon for ultra-shallow junction formation. *Journal of Applied Physics*, **2018**, 123, 125704	2.5	4
33	Electromechanical Diode Cell Scaling for High-Density Nonvolatile Memory. *IEEE Transactions on Electron Devices*, **2014**, 61, 1382-1387	2.9	4
32	First Demonstration of Quasi-Planar Segmented-Channel MOSFET Design for Improved Scalability. *IEEE Transactions on Electron Devices*, **2012**, 59, 2273-2276	2.9	4
31	Variation Study and Implications for BJT-Based Thin-Body Capacitorless DRAM. *IEEE Electron Device Letters*, **2012**, 33, 312-314	4.4	4
30	MuGFET carrier mobility and velocity: Impacts of fin aspect ratio, orientation and stress **2010**,		4
29	Tri-gate bulk MOSFET design for improved robustness to random dopant fluctuations **2008**,		4
28	Impact of flash annealing on performance and reliability of high-κ metal-gate MOSFETs for sub-45 nm CMOS **2007**,		4
27	Sub-lithographic Patterning via Tilted Ion Implantation for Scaling Beyond the 7-nm Technology Node. *IEEE Transactions on Electron Devices*, **2017**, 64, 231-236	2.9	3
26	Rapid melt grown germanium gate photoMOSFET on a silicon waveguide **2013**,		3
25	SRAM yield enhancement with thin-BOX FD-SOI **2009**,		3
24	SRAM yield and performance enhancements with tri-gate bulk MOSFETs **2008**,		3
23	Ultra-Low-Voltage Operation of MEM Relays for Cryogenic Logic Applications **2019**,		3
22	Effects of oxygen-inserted layers and oxide capping layer on dopant activation for the formation of ultrashallow p-n junctions in silicon. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2018**, 36, 061211	1.3	3
21	Modeling Nanoelectromechanical Switches With Random Surface Roughness. *IEEE Transactions on Electron Devices*, **2017**, 64, 2409-2416	2.9	2
20	Simulation-Based Study of High-Density SRAM Voltage Scaling Enabled by Inserted-Oxide FinFET Technology. *IEEE Transactions on Electron Devices*, **2019**, 66, 1754-1759	2.9	2
19	Micro-relay reliability improvement by inkjet-printed microshell encapsulation **2013**,		2
18	Inkjet-printed micro-electro-mechanical switches **2011**,		2

17	Embedded Memory Capability of Four-Terminal Relay Technology. *IEEE Transactions on Electron Devices*, **2011**, 58, 891-894	2.9	2
16	SRAM design in fully-depleted SOI technology **2010**,		2
15	Full 3D Simulation of 6T-SRAM Cells for the 22nm Node **2009**,		2
14	Low-Standby-Power Bulk MOSFET Design Using High-k Trench Isolation. *IEEE Electron Device Letters*, **2009**, 30, 1380-1382	4.4	2
13	SRAM cell design considerations for SOI technology **2009**,		2
12	Comparative Study of FinFET Versus Quasi-Planar HTI MOSFET for Ultimate Scalability. *IEEE Transactions on Electron Devices*, **2010**, 57, 3250-3256	2.9	2
11	Reducing adhesion energy of micro-relay electrodes by ion beam synthesized oxide nanolayers. *APL Materials*, **2017**, 5, 036103	5.7	1
10	Electrical Characterization of Etch Rate for Micro- and Nano-Scale Gap Formation. *Journal of Microelectromechanical Systems*, **2010**, 19, 1260-1263	2.5	1
9	Impact of random telegraph signals on Vmin in 45nm SRAM **2009**,		1
8	WireFET Technology for 3-D Integrated Circuits **2006**,		1
7	Cell Ratio Tuning for High-Density SRAM Voltage Scaling With Inserted-Oxide FinFETs. *IEEE Electron Device Letters*, **2016**, 37, 1539-1542	4.4	1
6	Design optimization of sub-5 nm node nanosheet field effect transistors to minimize self-heating effects. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2021**, 39, 013201	1.3	1
5	Simulation-Based Study of Si/Si0.9Ge0.1/Si Hetero-Channel FinFET for Enhanced Performance in Low-Power Applications. *IEEE Electron Device Letters*, **2019**, 40, 363-366	4.4	0
4	Defect Passivation by Selenium-Ion Implantation for Poly-Si Thin Film Transistors. *IEEE Electron Device Letters*, **2007**, 28, 725-727	4.4	0
3	Breakdown and Healing of Tungsten-Oxide Films on Microelectromechanical Relay Contacts. *Journal of Microelectromechanical Systems*, **2022**, 1-10	2.5	0
2	NEMS Switch Technology **2014**, 370-389		
1	Tuning of Schottky barrier height using oxygen-inserted (OI) layers and fluorine implantation. *AIP Advances*, **2020**, 10, 065310	1.5	