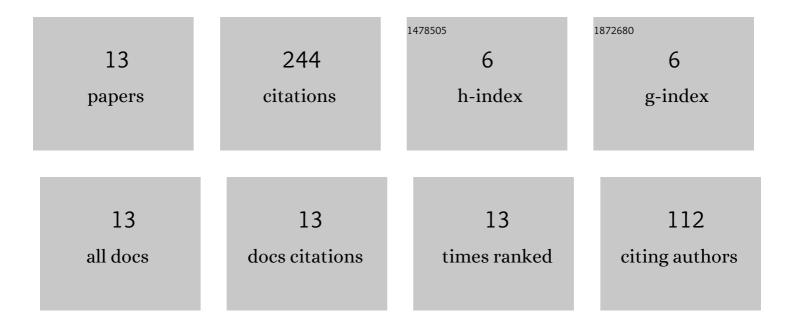
## Sadegh Yazdanshenas

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/2895164/publications.pdf Version: 2024-02-01



#	Article	IF	CITATIONS
1	FPGA Logic Block Architectures for Efficient Deep Learning Inference. ACM Transactions on Reconfigurable Technology and Systems, 2020, 13, 1-34.	2.5	19
2	The Costs of Confidentiality in Virtualized FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2272-2283.	3.1	18
3	COFFE 2. ACM Transactions on Reconfigurable Technology and Systems, 2019, 12, 1-27.	2.5	32
4	Math Doesn't Have to be Hard. , 2019, , .		9
5	Interconnect Solutions for Virtualized Field-Programmable Gate Arrays. IEEE Access, 2018, 6, 10497-10507.	4.2	20
6	Embracing Diversity: Enhanced DSP Blocks for Low-Precision Deep Learning on FPGAs. , 2018, , .		39
7	Improving Confidentiality in Virtualized FPGAs. , 2018, , .		5
8	You Cannot Improve What You Do not Measure. ACM Transactions on Reconfigurable Technology and Systems, 2018, 11, 1-23.	2.5	42
9	Don't Forget the Memory. , 2017, , .		16
10	Automatic circuit design and modelling for heterogeneous FPGAs. , 2017, , .		13
11	Quantifying and mitigating the costs of FPGA virtualization. , 2017, , .		14
12	High density, low energy, magnetic tunnel junction based block RAMs for memory-rich FPGAs. , 2016, , .		8
13	Fine-Grained Architecture in Dark Silicon Era for SRAM-Based Reconfigurable Devices. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 798-802.	3.0	9