Mary Hickson

List of Publications by Year in Descending Order

33 papers	97 citations	5 h-index	8 g-index
49 ext. papers	135 ext. citations	1.3 avg, IF	2.7 L-index

#	Paper	IF	Citations
33	Efficient half-precision floating point multiplier targeting color space conversion. *Multimedia Tools and Applications*, **2020**, 79, 89-117	2.5	2
32	High-Throughput Deblocking Filter Architecture Using Quad Parallel Edge Filter for H.264 Video Coding Systems. *IEEE Access*, **2019**, 7, 99642-99650	3.5	3
31	Two-stage low power test data compression for digital VLSI circuits. *Computers and Electrical Engineering*, **2018**, 71, 309-320	4.3	5
30	The Mediating Role of Overall Equipment Effectiveness on the Relationship between Fit Manufacturing and Business Performance. *International Journal of Engineering and Technology(UAE)* , **2018**, 7, 1089	0.8	2
29	Standby and dynamic power minimization using enhanced hybrid power gating structure for deep-submicron CMOS VLSI. *Microelectronics Journal*, **2017**, 62, 137-145	1.8	10
28	An area-efficient 32-bit floating point multiplier using hybrid GPPs addition **2017**,		1
27	A SAD architecture for variable block size motion estimation in H.264 video coding **2017**,		1
26	Monte-Carlo Black-Scholes Implementation using OpenCL Standard. *Indian Journal of Science and Technology*, **2016**, 9, 1-5	1	2
25	OBJECT TRACKING ALGORITHM IMPLEMENTATION FOR SECURITY APPLICATIONS. *Far East Journal of Electronics and Communications*, **2016**, 16, 1-13	0	11
24	Voice Controlled Energy Management System. *Asian Journal of Applied Sciences*, **2016**, 10, 25-31	0.4	
23	An Efficient Single Precision Floating Point Multiplier Architecture based on Classical Recoding Algorithm. *Indian Journal of Science and Technology*, **2016**, 9,	1	1
22	An Efficient Algorithm for Tracing Minimum Leakage Current Vector in Deep-Sub Micron Circuits. *Advances in Intelligent Systems and Computing*, **2016**, 59-69	0.4	1
21	FPGA implementation of FFT blocks for OFDM **2015**,		2
20	Implementation of radix-4 butterfly structure to prevent arithmetic overflow **2015**,		1
19	Study of approximate compressors for multiplication using FPGA **2015**,		3
18	VLSI implementation of fast convolution **2015**,		1
17	Design and implementation of 16□16 modified booth multiplier **2015**,		3

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16	Face detection system using FPGA **2015**,		2
15	Sine and cosine generator using CORDIC algorithm implemented in ASIC **2015**,		1
14	Implementation of Blake 256 hash function for password encryption and parallel CRC **2015**,		1
13	Home automation through FPGA controller **2015**,		2
12	Energy conservation using automatic lighting system using FPGA **2015**,		3
11	FPGA implementation of edge detection using Canny algorithm **2015**,		2
10	Dynamic Reconfigurable Architectures A Boon for Desires of Real Time Systems. *Advances in Intelligent Systems and Computing*, **2015**, 235-244	0.4	
9	Implementation of Special Function Unit for Vertex Shader Processor Using Hybrid Number System. *Journal of Computer Networks and Communications*, **2014**, 2014, 1-7	2.5	
8	Low-power selective pattern compression for scan-based test applications. *Computers and Electrical Engineering*, **2014**, 40, 1053-1063	4.3	5
7	Enhancement of test data compression with multistage encoding. *The Integration VLSI Journal*, **2014**, 47, 499-509	1.4	11
6	Adaptive Low Power RTPG for BIST based test applications **2013**,		1
5	Reduction of Test Power and Test Data Volume by Power Aware Compression Scheme **2012**,		3
4	CSP-Filling: A New X-Filling Technique to Reduce Capture and Shift Power in Test Applications **2012** ,		2
3	Reduction of testing power with pulsed scan flip-flop for scan based testing **2011**,		2
2	A novel approach for simultaneous reduction of shift and capture power for scan based testing **2011**,		4
1	Low power reconfigurable multiplier with reordering of partial products **2011**,		3