Mary Hickson

List of Publications by Year
in descending order

42 papers	187 citations	1684188 5 h-index	1474206 9 g-index
49 all docs	49 docs citations	49 times ranked	137 citing authors

#	Article	IF	Citations
1	OBJECT TRACKING ALGORITHM IMPLEMENTATION FOR SECURITY APPLICATIONS. Far East Journal of Electronics and Communications, 2016, 16, 1-13.	0.2	17
2	Enhancement of test data compression with multistage encoding. The Integration VLSI Journal, 2014, 47, 499-509.	2.1	14
3	Standby and dynamic power minimization using enhanced hybrid power gating structure for deep-submicron CMOS VLSI. Microelectronics Journal, 2017, 62, 137-145.	2.0	12
4	Two-stage low power test data compression for digital VLSI circuits. Computers and Electrical Engineering, 2018, 71, 309-320.	4.8	9
5	Design and implementation of 16Ã—16 modified booth multiplier. , 2015, , .		8
6	A novel approach for simultaneous reduction of shift and capture power for scan based testing. , 2011, , .		7
7	Low-power selective pattern compression for scan-based test applications. Computers and Electrical Engineering, 2014, 40, 1053-1063.	4.8	7
8	Energy conservation using automatic lighting system using FPGA. , 2015, , .		7
9	Low power reconfigurable multiplier with reordering of partial products. , 2011, , .		6
10	Reduction of Test Power and Test Data Volume by Power Aware Compression Scheme. , 2012, , .		5
11	Adaptive Low Power RTPG for BIST based test applications. , 2013, , .		5
12	Study of approximate compressors for multiplication using FPGA. , 2015, , .		5
13	Sine and cosine generator using CORDIC algorithm implemented in ASIC. , 2015, , .		5
14	Implementation of Blake 256 hash function for password encryption and parallel CRC. , 2015, , .		5
15	FPGA implementation of edge detection using Canny algorithm. , 2015, , .		5
16	An Efficient Single Precision Floating Point Multiplier Architecture based on Classical Recoding Algorithm. Indian Journal of Science and Technology, 2016, 9, .	0.7	5
17	Reduction of testing power with pulsed scan flip-flop for scan based testing. , 2011, , .		4
18	CSP-Filling: A New X-Filling Technique to Reduce Capture and Shift Power in Test Applications. , 2012, , .		4

#	Article	IF	Citations
19	Face detection system using FPGA. , 2015, , .		4
20	Home automation through FPGA controller. , 2015, , .		4
21	High-Throughput Deblocking Filter Architecture Using Quad Parallel Edge Filter for H.264 Video Coding Systems. IEEE Access, 2019, 7, 99642-99650.	4.2	4
22	Efficient half-precision floating point multiplier targeting color space conversion. Multimedia Tools and Applications, 2020, 79, 89-117.	3.9	4
23	The Mediating Role of Overall Equipment Effectiveness on the Relationship between Fit Manufacturing and Business Performance. International Journal of Engineering and Technology(UAE), 2018, 7, 1089.	0.3	4
24	FPGA implementation of FFT blocks for OFDM. , 2015, , .		3
25	Implementation of radix-4 butterfly structure to prevent arithmetic overflow. , 2015, , .		3
26	FPGA implementation of universal asynchronous transmitter and receiver. , 2015, , .		3
27	Image edge detection in FPGA. , 2015, , .		3
28	Modeling and Test Generation for Combinational Hardware Trojans. , 2020, , .		3
29	Partial Reconfigurable Implementation of IEEE802.11g OFDM. Indian Journal of Science and Technology, 2014, 7, 63-70.	0.7	3
30	Monte-Carlo Black-Scholes Implementation using OpenCL Standard. Indian Journal of Science and Technology, 2016, 9, 1-5.	0.7	3
31	Adaptive test clock scheme for low transition LFSR and external scan based testing. , 2013, , .		2
32	VLSI implementation of fast convolution. , 2015, , .		2
33	Fused floating-point add and subtract unit. , 2015, , .		2
34	A SAD architecture for variable block size motion estimation in H.264 video coding. , 2017, , .		2
35	Implementation of Special Function Unit for Vertex Shader Processor Using Hybrid Number System. Journal of Computer Networks and Communications, 2014, 2014, 1-7.	1.6	1
36	An area-efficient 32-bit floating point multiplier using hybrid GPPs addition. , 2017, , .		1

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37	ASIC Design of Reversible Adder and Multiplier. International Journal of Computer Applications, 2015, 109, 6-10.	0.2	1
38	Verilog implementation of fully pipelined and multiplierless 2D DCT/IDCT JPEG architecture. , 2015, , .		0
39	A reconfigurable coprocessor units with redundant radix-4 arithmetic. , 2015, , .		0
40	A face detection system implemented on FPGA based on RCT colour segmentation. , 2016, , .		0
41	Implementation of Hierarchical DFT Approach for Better Testability. , 2018, , .		0
42	Voice Controlled Energy Management System. Asian Journal of Applied Sciences, 2016, 10, 25-31.	0.4	0