Ãngel Benito RodrÃ-guez VÃ¡zquez

List of Publications by Year
in descending order

145 papers	2,363 citations	279798 23 h-index	276875 41 g-index
155 all docs	155 docs citations	155 times ranked	1372 citing authors

#	Article	IF	Citations
1	An Efficient TDC Using a Dual-Mode Resource-Saving Method Evaluated in a 28-nm FPGA. IEEE Transactions on Instrumentation and Measurement, 2022, 71, 1-13.	4.7	6
2	A Mobile Platform for Movement Tracking Based on a Fast-Execution-Time Optical-Flow Algorithm. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1715-1727.	5.4	1
3	Architecture-Level Optimization on Digital Silicon Photomultipliers for Medical Imaging. Sensors, 2022, 22, 122.	3.8	2
4	Design of High-Efficiency SPADs for LiDAR Applications in 110nm CIS Technology. IEEE Sensors Journal, 2021, 21, 4776-4785.	4.7	16
5	On the Virtualization of ISCAS 2020 Seville: For Real [Society News]. IEEE Circuits and Systems Magazine, 2021, 21, 81-84.	2.3	1
6	A 32-Channel Time-Multiplexed Artifact-Aware Neural Recording System. IEEE Transactions on Biomedical Circuits and Systems, 2021, 15, 960-977.	4.0	11
7	Compressive Imaging Using RIP-Compliant CMOS Imager Architecture and Landweber Reconstruction. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 387-399.	8.3	14
8	Offset-Calibration With Time-Domain Comparators Using Inversion-Mode Varactors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 47-51.	3.0	6
9	Comparison between Digital Tone-Mapping Operators and a Focal-Plane Pixel-Parallel Circuit. Signal Processing: Image Communication, 2020, 88, 115937.	3.2	0
10	A comparative study of stacked-diode configurations operating in the photovoltaic region. IEEE Sensors Journal, 2020, , 1-1.	4.7	9
11	Charge-redistribution based quadratic operators for neural feature extraction. IEEE Transactions on Biomedical Circuits and Systems, 2020, 14, 1-1.	4.0	5
12	Compact Macro-Cell With OR Pulse Combining for Low Power Digital-SiPM. IEEE Sensors Journal, 2020, 20, 12817-12826.	4.7	1
13	A Sub-mu W Reconfigurable Front-End for Invasive Neural Recording That Exploits the Spectral Characteristics of the Wideband Neural Signal. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1426-1437.	5.4	16
14	PreVIous: A Methodology for Prediction of Visual Inference Performance on IoT Devices. IEEE Internet of Things Journal, 2020, 7, 9227-9240.	8.7	15
15	Performance Assessment of Deep Learning Frameworks through Metrics of CPU Hardware Exploitation on an Embedded Platform. International Journal of Electrical and Computer Engineering Systems, 2020, 11, 1-11.	0.6	1
16	Phase Synchronization Operator for On-Chip Brain Functional Connectivity Computation. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 957-970.	4.0	8
17	Guest Editorial: Special Section on the 48th European Solid-State Circuits Conference (ESSCIRC). IEEE Journal of Solid-State Circuits, 2019, 54, 1827-1829.	5.4	0
18	Artifact-Aware Analogue/Mixed-Signal Front-Ends for Neural Recording Applications. , 2019, , .		2

#	Article	IF	Citations
19	Characterization-Based Modeling of Retriggering and Afterpulsing for Passively Quenched CMOS SPADs. IEEE Sensors Journal, 2019, 19, 5700-5709.	4.7	11
20	A 32 Input Multiplexed Channel Analog Front-End with Spatial Delta Encoding Technique and Differential Artifacts Compression. , 2019, , .		4
21	Optimum Selection of DNN Model and Framework for Edge Inference. IEEE Access, 2018, 6, 51680-51692.	4.2	16
22	On the Analysis and Detection of Flames With an Asynchronous Spiking Image Sensor. IEEE Sensors Journal, 2018, 18, 6588-6595.	4.7	9
23	Asynchronous Spiking Pixel With Programmable Sensitivity to Illumination. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3854-3863.	5.4	0
24	Applications of eventâ€based image sensorsâ€”Review and analysis. International Journal of Circuit Theory and Applications, 2018, 46, 1620-1630.	2.0	14
25	System-Level Design of a 64-Channel Low Power Neural Spike Recording Sensor. IEEE Transactions on Biomedical Circuits and Systems, 2017, 11, 420-433.	4.0	25
26	A Wide Linear Dynamic Range Image Sensor Based on Asynchronous Self-Reset and Tagging of Saturation Events. IEEE Journal of Solid-State Circuits, 2017, 52, 1605-1617.	5.4	15
27	Arrayable Voltage-Controlled Ring-Oscillator for Direct Time-of-Flight Image Sensors. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2821-2834.	5.4	32
28	A switchedâ€capacitor skewâ€tent map implementation for random number generation. International Journal of Circuit Theory and Applications, 2017, 45, 305-315.	2.0	45
29	Sun Sensor Based on a Luminance Spiking Pixel Array. IEEE Sensors Journal, 2017, 17, 6578-6588.	4.7	11
30	Gaussian Pyramid: Comparative Analysis of Hardware Architectures. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2308-2321.	5.4	3
31	Low-Power CMOS Vision Sensor for Gaussian Pyramid Extraction. IEEE Journal of Solid-State Circuits, 2017, 52, 483-495.	5.4	23
32	Compact CMOS active quenching/recharge circuit for SPAD arrays. International Journal of Circuit Theory and Applications, 2016, 44, 917-928.	2.0	10
33	Integer-based digital processor for the estimation of phase synchronization between neural signals. , 2016, , .		2
34	Image Sensing Scheme Enabling Fully-Programmable Light Adaptation and Tone Mapping With a Single Exposure. IEEE Sensors Journal, 2016, 16, 5121-5122.	4.7	3
35	Image Feature Extraction Acceleration. Studies in Computational Intelligence, 2016, , 109-132.	0.9	1
36	Time interval generator with 8Âps resolution and wide range for large TDC array characterization. Analog Integrated Circuits and Signal Processing, 2016, 87, 181-189.	1.4	15

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37	Bottomâ€up performance analysis of focalâ€plane mixedâ€signal hardware for Violaâ€“Jones early vision tasks. International Journal of Circuit Theory and Applications, 2015, 43, 1063-1079.	2.0	7
38	CMOS image sensor architecture for focal plane early vision processing. , 2015, , .		0
39	A 64-channel ultra-low power system-on-chip for local field and action potentials recording. Proceedings of SPIE, 2015, , .	0.8	0
40	Focal-Plane Sensing-Processing: A Power-Efficient Approach for the Implementation of Privacy-Aware Networked Visual Sensors. Sensors, 2014, 14, 15203-15226.	3.8	15
41	Form factor improvement of smart-pixels for vision sensors through 3-D vertically-integrated technologies. , 2014, , .		1
42	Equalization-Based Digital Background Calibration Technique for Pipelined ADCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 322-333.	3.1	25
43	Review of ADCs for imaging. Proceedings of SPIE, 2014, , .	0.8	4
44	A 330μW, 64-channel neural recording sensor with embedded spike feature extraction and auto-calibration. , 2014, , .		2
45	A battery-free 64-channel neural spike wireless sensor array. , 2013, , .		0
46	Special Issue on Advances in sensing and communication circuits (ICECS 2012). Analog Integrated Circuits and Signal Processing, 2013, 77, 315-317.	1.4	0
47	A tone mapping algorithm for acquisition of high dynamic range images using event-driven adaptive digital CMOS pixels. Analog Integrated Circuits and Signal Processing, 2013, 77, 401-413.	1.4	0
48	A hierarchical vision processing architecture oriented to 3D integration of smart camera chips. Journal of Systems Architecture, 2013, 59, 908-919.	4.3	9
49	High-speed global shutter CMOS machine vision sensor with high dynamic range image acquisition and embedded intelligence. , 2012, , .		1
50	Early forest fire detection by vision-enabled wireless sensor networks. International Journal of Wildland Fire, 2012, 21, 938.	2.4	38
51	CMOS-3D Smart Imager Architectures for Feature Detection. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2012, 2, 723-736.	3.6	19
52	Ultralow-Power Processing Array for Image Enhancement and Edge Detection. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 751-755.	3.0	9
53	Real-time remote reporting of motion analysis with Wi-FLIP. , 2012, , .		0
54	A 1.2ÂV 10-bit 60-MS/s 23ÂmW CMOS pipeline ADC with 0.67ÂpJ/conversion-step and on-chip reference voltages generator. Analog Integrated Circuits and Signal Processing, 2012, 71, 371-381.	1.4	7

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55	A Low-Power Programmable Neural Spike Detection Channel With Embedded Calibration and Data Compression. IEEE Transactions on Biomedical Circuits and Systems, 2012, 6, 87-100.	4.0	94
56	ICâ€constrained optimization of continuousâ€time Gmâ€“C filters. International Journal of Circuit Theory and Applications, 2012, 40, 127-143.	2.0	7
57	Behavioral modeling of pipeline ADC building blocks. International Journal of Circuit Theory and Applications, 2012, 40, 571-594.	2.0	6
58	Transistor-Level Synthesis of Pipeline Analog-to-Digital Converters Using a Design-Space Reduction Algorithm. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2816-2828.	5.4	13
59	A self-calibration circuit for a neural spike recording channel. , 2011, , .		8
60	Wi-FLIP: A wireless smart camera based on a focal-plane low-power image processor. , 2011, , .		9
61	Introduction to the Special Issue on the 36th European Solid-State Circuits Conference (ESSCIRC). IEEE Journal of Solid-State Circuits, 2011, 46, 1519-1521.	5.4	0
62	An auto-calibrated neural spike recording channel with feature extraction capabilities. Proceedings of SPIE, 2011, , .	0.8	1
63	Demo: Real-time remote reporting of active regions with Wi-FLIP. , 2011, , .		0
64	A power efficient neural spike recording channel with data bandwidth reduction. , 2011, , .		1
65	VISCUBE: A Multi-Layer Vision Chip. , 2011, , 181-208.		3
66	A Focal Plane Processor for Continuous-Time 1-D Optical Correlation Applications. , 2011, , 151-179.		0
67	Offset-compensated comparator with full-input range in 150nm FDSOI CMOS-3D technology. , 2010, , .		2
68	In-pixel ADC for a vision architecture on CMOS-3D technology. , 2010, , .		5
69	A 3D chip architecture for optical sensing and concurrent processing. Proceedings of SPIE, 2010, , .	0.8	6
70	Digital processor array implementation aspects of a 3D multi-layer vision architecture. , 2010, , .		3
71	ESSCIRC and ESSDERC, 13â€“17 September 2010, Seville, Spain [Conference Reports]. IEEE Solid-State Circuits Magazine, 2010, 2, 81-81.	0.4	0
72	A CMOS vision system on-chip with multicore sensory processing architecture for image analysis above 1,000F/s. , 2010, , .		3

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73	Transformer based front-end for a low power 2.4 GHz transceiver. , 2010, , .		5
74	Baseband-processor for a passive UHF RFID transponder. , 2010, , .		2
75	A CMOS Vision System On-Chip with Multi-Core, Cellular Sensory-Processing Front-End. , 2010, , 129-146.		26
76	3D multi-layer vision architecture for surveillance and reconnaissance applications. , 2009, , .		8
77	ECCTD 2007 Special Issue â€˜Bridging Technology Innovations to Foundationsâ€™. International Journal of Circuit Theory and Applications, 2009, 37, 159-161.	2.0	0
78	Accurate Settling-Time Modeling and Design Procedures for Two-Stage Miller-Compensated Amplifiers for Switched-Capacitor Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1077-1087.	5.4	30
79	A low-power reconfigurable ADC for biomedical sensor interfaces. , 2009, , .		7
80	Clock jitter error in multi-bit continuous-time sigma-delta modulators with non-return-to-zero feedback waveform. Microelectronics Journal, 2008, 39, 137-151.	2.0	5
81	Electrical-level synthesis of pipeline ADCs. , 2008, , .		0
82	Insect-vision inspired collision warning vision processor for automobiles. IEEE Circuits and Systems Magazine, 2008, 8, 6-24.	2.3	11
83	Matrix Methods for the Dynamic Range Optimization of Continuous-Time G_{m}-C Filters. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2525-2538.	5.4	8
84	CMOS architectures and circuits for high-speed decision-making from image flows. , 2008, , .		1
85	The Eye-RIS CMOS Vision System. , 2008, , 15-32.		38
86	Systematic Design of High-Resolution High-Frequency Cascade Continuous-Time Sigma-Delta Modulators. ETRI Journal, 2008, 30, 535-545.	2.0	1
87	A 12-bit@40MS/s Gm-C Cascade 3-2 Continuous-Time Sigma-Delta Modulator. , 2007, , .		3
88	Accurate and simple modeling of amplifier dc gain nonlinearity in switched-capacitor circuits. , 2007, , .		5
89	A 5.3mW, 2.4GHz ESD protected Low-Noise Amplifier in a 0.13μm RFCMOS technology. , 2007, , .		2
90	Early slip detection with a tactile sensor based on retina. Analog Integrated Circuits and Signal Processing, 2007, 53, 97-108.	1.4	9

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91	Bio-inspired 0.35Â¿m CMOS Time-to-Digital Converter with 29.3ps LSB. Solid-State Circuits Conference, 2008 ESSCIRC 2008 34th European, 2006, , .	0.0	1
92	<title>ACE16k based stand-alone system for real-time pre-processing tasks</title>. , 2005, , .		7
93	<title>A 0.18-Î¼m CMOS low-noise highly linear continuous-time seventh-order elliptic low-pass filter</title>. , 2005, , .		1
94	<title>Continuous-time cascaded Î£Î” modulators for VDSL: a comparative study</title>. , 2005, , .		0
95	<title>A 0.35-Î¼m CMOS 17-bit@40-kS/s cascade 2-1 Î£Î” modulator with programmable gain and programmable chopper stabilization</title>. , 2005, , .		0
96	<title>Simulation-based high-level synthesis of Nyquist-rate data converters using MATLAB/SIMULINK</title>. , 2005, 5837, 235.		1
97	A CMOS 110-dB@40-kS/s programmable-gain chopper-stabilized third-order 2-1 cascade sigma-delta Modulator for low-power high-linearity automotive sensor ASICs. IEEE Journal of Solid-State Circuits, 2005, 40, 2246-2264.	5.4	34
98	A mixed-signal integrated circuit for FM-DCSK modulation. IEEE Journal of Solid-State Circuits, 2005, 40, 1460-1471.	5.4	16
99	Analysis of Error Mechanisms in Switched-Current Sigma-Delta Modulators. Analog Integrated Circuits and Signal Processing, 2004, 38, 175-201.	1.4	9
100	Synthesis of a Wireless Communication Analog Back-End Based on a Mismatch-Aware Symbolic Approach. Analog Integrated Circuits and Signal Processing, 2004, 40, 215-233.	1.4	1
101	Bio-Inspired Nano-Sensor-Enhanced CNN Visual Computer. Annals of the New York Academy of Sciences, 2004, 1013, 92-109.	3.8	19
102	A 1000 FPS at 128/spl times/128 vision processor with 8-bit digitized I/O. IEEE Journal of Solid-State Circuits, 2004, 39, 1044-1055.	5.4	70
103	Mismatch-Induced Trade-Offs and Scalability of Analog Preprocessing Visual Microprocessor Chips. Analog Integrated Circuits and Signal Processing, 2003, 37, 73-83.	1.4	5
104	Mixed-signal early vision chip with embedded image and programming memories and digital I/O. , 2003, 5117, 379.		0
105	Programmable retinal dynamics in a CMOS mixed-signal array processor chip. , 2003, 5119, 13.		3
106	A bio-inspired two-layer mixed-signal flexible programmable chip for early vision. IEEE Transactions on Neural Networks, 2003, 14, 1313-1336.	4.2	41
107	Neuro-fuzzy chip to handle complex tasks with analog performance. IEEE Transactions on Neural Networks, 2003, 14, 1375-1392.	4.2	12
108	EXPLORATION OF SPATIAL-TEMPORAL DYNAMIC PHENOMENA IN A 32Ã—32-CELL STORED PROGRAM TWO-LAYER CNN UNIVERSAL MACHINE CHIP PROTOTYPE. Journal of Circuits, Systems and Computers, 2003, 12, 691-710.	1.5	14

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109	ACE16k: A 128Ã—128 FOCAL PLANE ANALOG PROCESSOR WITH DIGITAL I/O. International Journal of Neural Systems, 2003, 13, 427-434.	5.2	48
110	AN IMPROVED ELEMENTARY PROCESSING UNIT FOR HIGH-DENSITY CNN-BASED MIXED-SIGNAL MICROPROCESSORS FOR VISION. Journal of Circuits, Systems and Computers, 2003, 12, 675-690.	1.5	0
111	Î£-Î” modulator for a programmable gain, low-power, high-linearity automotive sensor interface. , 2003, , .		0
112	Toward a computational approach for collision avoidance with real-world scenes. , 2003, 5119, 285.		1
113	System-level optimization of baseband filters for communication applications. , 2003, , .		2
114	Versatile sensor interface for programmable vision systems-on-chip. , 2003, , .		1
115	CMOS mixed-signal MODEM for data transmission and control of electrical household appliances using the low-voltage power line. , 2003, , .		0
116	Practical study of idle tones in 2nd-order bandpass Î£Î” modulators. Microelectronics Journal, 2002, 33, 1005-1009.	2.0	1
117	A Symbolic Pole/Zero Extraction Methodology Based on Analysis of Circuit Time-Constants. Analog Integrated Circuits and Signal Processing, 2002, 31, 101-118.	1.4	15
118	Approximate Symbolic Analysis of Hierarchically Decomposed Analog Circuits. Analog Integrated Circuits and Signal Processing, 2002, 31, 131-145.	1.4	27
119	Generation of Technology-Independent Retargetable Analog Blocks. Analog Integrated Circuits and Signal Processing, 2002, 33, 157-170.	1.4	15
120	Title is missing!. Analog Integrated Circuits and Signal Processing, 2002, 33, 179-190.	1.4	19
121	Switched-Current bandpass Sigmaâ€“Delta modulators for AM digital radio receivers. Microelectronics Journal, 2001, 32, 1017-1033.	2.0	1
122	Reliable analysis of settling errors in SC integrators: application to modulators. Electronics Letters, 2000, 36, 503.	1.0	24
123	A CMOS 0.8-/spl mu/m transistor-only 1.63-MHz switched-current bandpass /spl Sigma//spl Delta/ modulator for AM signal A/D conversion. IEEE Journal of Solid-State Circuits, 2000, 35, 1220-1226.	5.4	8
124	A design approach for analog neuro/fuzzy systems in CMOS digital technologies. Computers and Electrical Engineering, 1999, 25, 309-337.	4.8	11
125	An 0.5-Î¼m CMOS analog random access memory chip for TeraOPS speed multimedia video processing. IEEE Transactions on Multimedia, 1999, 1, 121-135.	7.2	15
126	A 13-bit, 2.2-MS/s, 55-mW multibit cascade Î£Î” modulator in CMOS 0.7-Î¼m single-poly technology. IEEE Journal of Solid-State Circuits, 1999, 34, 748-760.	5.4	49

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127	Electrooptical measurement system for the DC characterization of visible detectors for CMOS-compatible vision chips. IEEE Transactions on Instrumentation and Measurement, 1998, 47, 499-506.	4.7	4
128	Theory, design and applications of Cellular Neural Networks. International Journal of Circuit Theory and Applications, 1998, 26, 549-549.	2.0	0
129	A 0.8-Î¼m CMOS two-dimensional programmable mixed-signal focal-plane array processor with on-chip binary imaging and instructions storage. IEEE Journal of Solid-State Circuits, 1997, 32, 1013-1026.	5.4	134
130	Using CAD tools for shortening the design cycle of high-performance sigmaâ€“delta modulators: A 16Â·4 bit, 9Â·6 kHz, 1Â·71 mW Î£Î”M in CMOS 0Â·7 Î¼m technology. International Journal of Circuit Theory and Applications, 1997, 25, 319-334.	2.0	13
131	<title>Mixed-signal CNN array chips for image processing</title>. , 1996, 2950, 218.		5
132	Efficient symbolic computation of approximated small-signal characteristics of analog integrated circuits. IEEE Journal of Solid-State Circuits, 1995, 30, 327-330.	5.4	71
133	CMOS optical-sensor array with high output current levels and automatic signal-range centring. Electronics Letters, 1994, 30, 1847-1849.	1.0	10
134	Smart-pixel cellular neural networks in analog current-mode CMOS technology. IEEE Journal of Solid-State Circuits, 1994, 29, 895-905.	5.4	59
135	Tunable feedthrough cancellation in switched-current circuits. Electronics Letters, 1994, 30, 1912-1914.	1.0	2
136	A CMOS analog adaptive BAM with on-chip learning and weight refreshing. IEEE Transactions on Neural Networks, 1993, 4, 445-455.	4.2	49
137	A modular T-mode design approach for analog neural network hardware implementations. IEEE Journal of Solid-State Circuits, 1992, 27, 701-713.	5.4	32
138	Analog neural programmable optimizers in CMOS VLSI technologies. IEEE Journal of Solid-State Circuits, 1992, 27, 1110-1115.	5.4	4
139	CMOS OTA-C high-frequency sinusoidal oscillators. IEEE Journal of Solid-State Circuits, 1991, 26, 160-165.	5.4	55
140	A CMOS implementation of FitzHugh-Nagumo neuron model. IEEE Journal of Solid-State Circuits, 1991, 26, 956-965.	5.4	114
141	On the design of voltage-controlled sinusoidal oscillators using OTAs. IEEE Transactions on Circuits and Systems, 1990, 37, 198-211.	0.9	111
142	Nonlinear switched capacitor 'neural' networks for optimization problems. IEEE Transactions on Circuits and Systems, 1990, 37, 384-398.	0.9	244
143	Analysis and design of selfâ€limiting singleâ€OPâ€AMPRC oscillators. International Journal of Circuit Theory and Applications, 1990, 18, 53-69.	2.0	9
144	Operational transconductance amplifier-based nonlinear function syntheses. IEEE Journal of Solid-State Circuits, 1989, 24, 1576-1586.	5.4	138

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145	A new nonlinear time-domain op-amp macromodel using threshold functions and digitally controlled network elements. IEEE Journal of Solid-State Circuits, 1988, 23, 959-971.	5.4	20