Haruo Kobayashi

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/2869307/publications.pdf

Version: 2024-02-01

115 papers	519 citations	1478505 6 h-index	1125743 13 g-index
116 all docs	116 docs citations	116 times ranked	223 citing authors

#	Article	IF	Citations
1	IEEE754 Binary32 Floating-Point Logarithmic Algorithms based on Taylor-Series Expansion with Mantissa Region Conversion and Division. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2022, , .	0.3	0
2	Metallic Ratio Equivalent-Time Sampling and Application to TDC Linearity Calibration. IEEE Transactions on Device and Materials Reliability, 2022, 22, 142-153.	2.0	2
3	Revisit to Histogram Method for ADC Linearity Test: Examination of Input Signal and Ratio of Input and Sampling Frequencies. Journal of Electronic Testing: Theory and Applications (JETTA), 2022, 38, 21-38.	1.2	4
4	Notch Frequency Generation Methods in Noise Spread Spectrum for Pulse Coding Switching DC-DC Converter. , 2022, , .		0
5	Study of analog-to-digital mixed integrated circuit configuration using number theory. Impact, 2022, 2022, 9-11.	0.1	0
6	Floating-Point Inverse Square Root Algorithm Based on Taylor-Series Expansion. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2640-2644.	3.0	5
7	Study of Rauch Low-Pass Filters using Pascal's Triangle. , 2021, , .		1
8	Limitations of Loop Gain in Motion Models of Physical Systems. , 2021, , .		0
9	Study on Current-Driven IGBT Driver Circuit. , 2021, , .		1
10	Digital-to-Analog Converter Configuration Based on Non-uniform Current Division Resistive-Ladder. , 2021, , .		4
11	Investigation of Behaviours of Kerwin-Huelsman-Newcomb Filters Using Nichols Charts of Self-Loop Function. , 2021, , .		0
12	Study of Helix Functions and Multi-Source Rauch Filters. , 2021, , .		1
13	Classical Mathematics and Analog/Mixed-Signal IC Design. , 2021, , .		0
14	Multi-Output SEIPC Multiplied Boost Converter with Exclusive Control. , 2021, , .		0
15	Revisit to Accurate ADC Testing with Incoherent Sampling Using Proper Sinusoidal Signal and Sampling Frequencies. , 2021, , .		3
16	Adaptive Convergence Method of Notch Frequency in Noise Spread Spectrum for Pulse Coding Switching DC-DC Converter. , 2021, , .		1
17	Analysis of Switching Characteristics of Wide SOA and High Reliability 100 V N-LDMOS Transistor with Dual RESURF and Grounded Field Plate Structure. , 2021, , .		1
18	Divide and Conquer: Floating-Point Exponential Calculation Based on Taylor-Series Expansion. , 2021, , .		1

#	Article	IF	Citations
19	Avidinâ€“Biotin Technology in Gold Nanoparticle-Decorated Graphene Field Effect Transistors for Detection of Biotinylated Macromolecules with Ultrahigh Sensitivity and Specificity. ACS Omega, 2020, 5, 30037-30046.	3.5	13
20	Activation Modeling and Classification of Voluntary and Imagery Movements From the Prefrontal fNIRS Signals. IEEE Access, 2020, 8, 218215-218233.	4.2	11
21	Graphene field-effect transistor biosensor for detection of biotin with ultrahigh sensitivity and specificity. Biosensors and Bioelectronics, 2020, 165, 112363.	10.1	70
22	Study of Behaviors of Electronic Amplifiers Using Nichols Chart. , 2020, , .		1
23	Ringing Test for Tow-Thomas Low-Pass Filters. , 2020, , .		1
24	Ringing Test for Second-Order Sallen-Key Low-Pass Filters. , 2020, , .		3
25	Pulse Coding Controlled Switching Converter that Generates Notch Frequency to Suit Noise Spectrum. IEICE Transactions on Communications, 2020, E103.B, 1331-1340.	0.7	5
26	Ringing Test for Third-Order Ladder Low-Pass Filters. , 2020, , .		4
27	Improved Nagata Current Source Insensitive to Temperature and Power Supply Voltage. , 2020, , .		3
28	Study on Crest Factor Controlled Multi-Tone Signal for Analog RF Circuit Testing. , 2020, , .		1
29	Nonlinearity Analysis of Resistive Ladder-Based Current-Steering Digital-to-Analog Converter. , 2020, , .		5
30	Low Power Loss IGBT Driver Circuit Using Current Drive. , 2020, , .		3
31	Design Of LC Harmonic Notch Filter for Ripple Reduction in Step-Down DC-DC Buck Converter. , 2020, , .		1
32	DESIGN OF SIXTH-ORDER PASSIVE QUADRATURE SIGNAL GENERATION NETWORK BASED ON POLYPHASE FILTER. , 2020, , .		1
33	Analog/Mixed-Signal Circuit Testing Technologies in IoT Era. , 2020, , .		10
34	Summing Node Test Method: Simultaneous Multiple AC Characteristics Testing of Multiple Operational Amplifiers. , 2020, , .		3
35	Analysis and Design of Multi-Tone Signal Generation Algorithms for Reducing Crest Factor. , 2020, , .		2
36	Measurements of Self-Loop Functions in High-Order Passive and Active Low-Pass Filters. , 2020, , .		1

#	Article	IF	Citations
37	Ringing Test for Negative Feedback Amplifiers. , 2020, , .		2
38	Multi-Phase Full/Half Wave Type Resonant Converters with Automatic Current Balance against Element Variation. , 2019, , .		1
39	Optimization of High Reliability and Wide SOA 100 V LDMOS Transistor with Low Specific On-Resistance. , 2019, , .		0
40	Minimum Output Ripple and Fixed Operating Frequency Based on Modulation Injection for COT Ripple Control Converter. , 2019, , .		1
41	EMI Noise Reduction and Output Ripple Cancellation for Full-Wave Type Soft-Switching Converter. , 2019, , .		1
42	Analysis and Evaluation Method of RC Polyphase Filter. , 2019, , .		3
43	Evaluation of Null Method for Operational Amplifier Short-Time Testing. , 2019, , .		4
44	Fine Time Resolution TDC Architectures -Integral and Delta-Sigma Types. , 2019, , .		5
45	Accurate and Fast Testing Technique of Operational Amplifier DC Offset Voltage in ÂµV-Order by DC-AC Conversion. , 2019, , .		7
46	Crest Factor Controlled Multi-Tone Signals for Analog/Mixed-Signal IC Testing. , 2019, , .		6
47	A Distortion Shaping Technique to Equalize Intermodulation Distortion Performance of Interpolating Arbitrary Waveform Generators in Automated Test Equipment. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 215-232.	1.2	4
48	Unified Methodology of Analog/Mixed-Signal IC Design Based on Number Theory. , 2018, , .		1
49	Low-Distortion Signal Generation for Analog/Mixed-Signal IC Testing Using Digital ATE Output Pin and BOST. , 2018, , .		0
50	Full Automatic Notch Generation in Noise Spectrum of Pulse Coding Controlled Switching Converter. , 2018, , .		4
51	Limit Cycle Suppression Technique Using Random Signal In Delta-Sigma DA Modulator. , 2018, , .		0
52	EMI Noise Reduction for PFC Converter with Improved Efficiency and High Frequency Clock. , 2018, , .		2
53	Integral-type Time-to-Digital Converter. , 2018, , .		2
54	Silicon Verification of Improved Nagata Current Mirrors. , 2018, , .		3

#	Article	IF	Citations
55	Wide SOA and High Reliability 60-100 V LDMOS Transistors with Low Switching Loss and Low Specific On-Resistance. , 2018, , .		6
56	Performance Improvement of Delta-Sigma ADC/DAC/TDC Using Digital Technique. , 2018, , .		4
57	Highly Efficient Waveform Acquisition Condition in Equivalent-Time Sampling System. , 2018, , .		16
58	A Study on Loop Gain Measurement Method Using Output Impedance in DC-DC Buck Converter. IEICE Transactions on Communications, 2018, E101.B, 1940-1948.	0.7	2
59	Analysis and Design of Operational Amplifier Stability Based on Routh-Hurwitz Stability Criterion. IEEJ Transactions on Electronics, Information and Systems, 2018, 138, 1517-1528.	0.2	4
60	Using Distortion Shaping Technique to Equalize ADC THD Performance Between ATEs. Journal of Electronic Testing: Theory and Applications (JETTA), 2017, 33, 295-303.	1.2	4
61	DAC linearity improvement with layout technique using magic and latin squares. , 2017, , .		7
62	Fundamental design tradeoff and performance limitation of electronic circuits based on uncertainty relationships. , 2017, , .		2
63	SAR TDC Architecture with Self-Calibration Employing Trigger Circuit. , 2017, , .		5
64	Architecture of high performance successive approximation time digitizer. , 2017, , .		3
65	SAR TDC architecture for one-shot timing measurement with full digital implementation. , 2017, , .		5
66	Constant on-time controlled four-phase buck converter via two ways of saw-tooth-wave circuit and PLL circuit. , 2017, , .		1
67	Noise spread spectrum with adjustable notch frequency in complex pulse coding controlled DC-DC converters. , 2017, , .		5
68	Estimation of circuit component values in buck converter using efficiency curve. , 2017, , .		4
69	Two-phase soft-switching DC-DC converter with voltage-mode resonant switch. , 2017, , .		3
70	Equivalence between Nyquist and Routh-Hurwitz stability criteria for operational amplifier design. , 2017, , .		5
71	Fibonacci sequence weighted SAR ADC as golden section search. , 2017, , .		2
72	SAR ADC Algorithm With Redundancy Using Pseudo-Silver-Ratio. IEEJ Transactions on Electronics, Information and Systems, 2017, 137, 222-228.	0.2	1

#	Article	IF	Citations
73	Stochastic TDC Architecture with Self-Calibration and its RTL Verification. IEEJ Transactions on Electronics, Information and Systems, 2017, 137, 335-341.	0.2	0
74	Optimization and analysis of high reliability 30â€“50V dual RESURF LDMOS. , 2016, , .		6
75	Limit cycle suppression technique using digital dither in delta sigma DA modulator. , 2016, , .		5
76	Comparator circuit automation by combination of game tree search and partial optimization. , 2016, , .		1
77	High-frequency low-distortion one-tone and two-tone signal generation using arbitrary waveform generator. , 2016, , .		9
78	Timing measurement BOST architecture with full digital circuit and self-calibration using characteristics variation positively for fine time resolution. , 2016, , .		7
79	I-Q signal generation techniques for communication IC testing and ATE systems. , 2016, , .		17
80	DAC linearity improvement algorithm with unit cell sorting based on magic square. , 2016, , .		7
81	Fundamental design consideration of sampling circuit. , 2016, , .		2
82	Successive approximation time-to-digital converter with vernier-level resolution. , 2016, , .		16
83	Using distortion shaping technique to equalize ADC THD performance between ATEs. , 2016, , .		10
84	Hysteretic controlled buck converter with switching frequency insensitive to input/output voltage ratio. , 2016, , .		6
85	Analog / mixed-signal circuit design based on mathematics. , 2016, , .		5
86	Study of Gray code input DAC using MOSFETs for glitch reduction. , 2016, , .		3
87	Single-inductor dual-output soft-switching converter with voltage-mode resonant switch. , 2016, , .		2
88	EMI Reduction Technique for Switching Converter by Spectrum Spread using Pseudo Analog Signal. IEEJ Transactions on Electronics, Information and Systems, 2016, 136, 43-49.	0.2	0
89	A Glitch-Free Time-to-Digital Converter Architecture Based on Gray Code. IEEJ Transactions on Electronics, Information and Systems, 2016, 136, 22-27.	0.2	0
90	Single-Inductor Dual-Output DC-DC Converter Design Using RC Ripple Regulator Method. IEEJ Transactions on Electronics, Information and Systems, 2016, 136, 101-107.	0.2	1

#	Article	IF	Citations
91	Study on Delta Sigma DA Modulator Performance Improvement Using Digital Dither. IEEJ Transactions on Electronics, Information and Systems, 2016, 136, 1767-1772.	0.2	0
92	SAR ADC design using Golden ratio weight algorithm. , 2015, , .		7
93	High-frequency low-distortion signal generation algorithm with arbitrary waveform generator. , 2015, , .		15
94	Flat passband gain design algorithm for 2nd-order RC polyphase filter. , 2015, , .		2
95	Linearity enhancement algorithms for I-Q signal generation â€" DWA and self-calibration techniques. , 2015, , .		0
96	Fibonacci sequence weighted SAR ADC algorithm and its DAC topology. , 2015, , .		5
97	Selectable notch frequencies of EMI spread spectrum using pulse modulation in switching converter. , 2015, , .		5
98	Comparator circuits automation by combination of distributed genetic algorithm and HSPICE optimization. , 2015, , .		4
99	Transient Response Improvement of DC-DC Buck Converter by a Slope Adjustable Triangular Wave Generator. IEICE Transactions on Communications, 2015, E98.B, 288-295.	0.7	1
100	A study on HCI induced gate leakage current model used for reliability simulations in 90nm n-MOSFETs. , 2015, , .		0
101	A gray code based time-to-digital converter architecture and its FPGA implementation. , 2015, , .		7
102	Self-Heat Characterizations and Modeling of Multifinger nMOSFETs for RF-CMOS Applications. IEEE Transactions on Electron Devices, 2015, 62, 2704-2709.	3.0	5
103	A CMOS PWM Transceiver Using Self-Referenced Edge Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1145-1149.	3.1	6
104	Phase noise measurement techniques using delta-sigma TDC. , 2014, , .		11
105	Dynamic performance improvement of DC-DC buck converter by slope adjustable triangular wave generator. , 2014, , .		3
106	Digital calibration algorithm for half-unary current-steering DAC for linearity improvement. , 2014, , .		4
107	Time-to-digital converter architecture with residue arithmetic and its FPGA implementation. , 2014, , .		6
108	A low-offset cascaded time amplifier with reconfigurable inter-stage connection. IEICE Electronics Express, 2014, 11, 20140203-20140203.	0.8	1

#	Article	IF	Citations
109	Analog/mixed-signal circuit design in nano CMOS era. IEICE Electronics Express, 2014, 11, 20142001-20142001.	0.8	8
110	Multi-bit Sigma-Delta TDC Architecture with Improved Linearity. Journal of Electronic Testing: Theory and Applications (JETTA), 2013, 29, 879-892.	1.2	14
111	Digital Compensation for Timing Mismatches in Interleaved ADCs. , 2013, , .		7
112	An Analysis of Stochastic Self-Calibration of TDC Using Two Ring Oscillators. , 2013, , .		6
113	Single inductor dual output switching converter using exclusive control method. , 2013, , .		4
114	Design methodology for determining the number of stages in a cascaded time amplifier to minimize area consumption. IEICE Electronics Express, 2013, 10, 20130289-20130289.	0.8	4
115	Two-Tone Signal Generation for ADC Testing. IEICE Transactions on Electronics, 2013, E96.C, 850-858.	0.6	10