Jens SparsÃ¸

List of Publications by Year
in descending order

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24 papers	353 citations	1684188 5 h-index	1720034 7 g-index
25 all docs	25 docs citations	25 times ranked	236 citing authors

#	Article	IF	Citations
1	Synchronizing Real-Time Tasks in Time-Triggered Networks. , 2021, , .		5
2	A time-predictable open-source TTEthernet end-system. Journal of Systems Architecture, 2020, 108, 101744.	4.3	11
3	Design and FPGA-implementation of Asynchronous Circuits Using Two-Phase Handshaking. , 2019, , .		11
4	A Time-predictable TTEthenet Node. , 2019, , .		0
5	Hardlock: Real-time multicore locking. Journal of Systems Architecture, 2019, 97, 467-476.	4.3	3
6	Scratchpad Memories with Ownership. , 2019, , .		3
7	A Multicore Processor for Time-Critical Applications. IEEE Design and Test, 2018, 35, 38-47.	1.2	12
8	Using dynamic partial reconfiguration of FPGAs in real-Time systems. Microprocessors and Microsystems, 2018, 61, 198-206.	2.8	10
9	A resource-efficient network interface supporting low latency reconfiguration of virtual circuits in time-division multiplexing networks-on-chip. Journal of Systems Architecture, 2017, 74, 1-13.	4.3	4
10	Timing Organization of a Real-Time Multicore Processor. , 2017, , .		1
11	A Controller for Dynamic Partial Reconfiguration in FPGA-Based Real-Time Systems. , 2017, , .		17
12	Avionics Applications on a Time-Predictable Chip-Multiprocessor. , 2016, , .		6
13	Argo: A Real-Time Network-on-Chip Architecture With an Efficient GALS Implementation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 479-492.	3.1	69
14	Message Passing on a Time-predictable Multicore Processor. , 2015, , .		9
15	Models of Communication for Multicore Processors. , 2015, , .		4
16	Interfacing hardware accelerators to a time-division multiplexing network-on-chip. , 2015, , .		4
17	The Argo NOC: Combining TDM and GALS. , 2015, , .		4
18	T-CREST: Time-predictable multi-core architecture for embedded systems. Journal of Systems Architecture, 2015, 61, 449-471.	4.3	151

#	Article	IF	Citations
19	Synthesis and layout of an asynchronous network-on-chip using Standard EDA tools. , 2014, , .		4
20	A Metaheuristic Scheduler for Time Division Multiplexed Networks-on-Chip. , 2014, , .		17
21	Open core protocol (OCP) clock domain crossing interfaces. , 2014, , .		0
22	Analytical derivation of traffic patterns in cache-coherent shared-memory systems. Microprocessors and Microsystems, 2011, 35, 632-642.	2.8	0
23	Analytical derivation of traffic patterns in shared memory architectures from Task Graphs. , 2009, , .		1
24	Synthesis of topology configurations and deadlock free routing algorithms for ReNoC-based systems-on-chip. , 2009, , .		7