Paula Agopian

List of Publications by Year
in descending order

192 papers	777 citations	840776 11 h-index	677142 22 g-index
192 all docs	192 docs citations	192 times ranked	505 citing authors

#	Article	IF	Citations
1	Design of operational transconductance amplifier with Gate-All-Around Nanosheet MOSFET using experimental data from room temperature to 200ÂÂ°C. Solid-State Electronics, 2022, 189, 108238.	1.4	1
2	Trade-off analysis between gm/ID and fT of nanosheet NMOS transistors with different metal gate stack at high temperature. Solid-State Electronics, 2022, 191, 108267.	1.4	0
3	Comparison between Low-Dropout Voltage Regulators Designed with Line and Nanowire Tunnel Field Effect Transistors using Experimental Data. Solid-State Electronics, 2022, , 108328.	1.4	1
4	Voltage gain improvement of the operational transconductance amplifier designed with silicon-on-insulator fin field effect transistor after being exposed to proton-irradiation. Semiconductor Science and Technology, 2021, 36, 035001.	2.0	1
5	Study of a Fringing Field Biosensor Tunnel-FET. ECS Journal of Solid State Science and Technology, 2021, 10, 017004.	1.8	2
6	Analysis of the ZTC-Point for Vertically Stacked Nanosheet pMOS Devices. , 2021, , .		0
7	Impact of Positive Charges in a Fringing Field Bio-Tunnel-FET Device with Source Underlap. , 2021, , .		0
8	Simple Analytical Modelling of an Electronically Tunable Potentiometer and Body Factor Influence. , 2021, , .		0
9	Evaluation of Dielectrically Modulated and Fringing Field Tunneling Field Effect Transistor Biosensors Devices. ECS Journal of Solid State Science and Technology, 2021, 10, 077001.	1.8	1
10	Analog Figures of Merit of Vertically Stacked Silicon Nanosheets nMOSFETs With Two Different Metal Gates for the Sub-7 nm Technology Node Operating at High Temperatures. IEEE Transactions on Electron Devices, 2021, 68, 3630-3635.	3.0	18
11	Current mirror designed with GAA nanosheet MOSFETs from room temperature to 200 Â°C. Semiconductor Science and Technology, 2021, 36, 095019.	2.0	1
12	The Impact of Spacer Oxide Material on the Underlapped SOI-nFinFET Working as Charged Based Radiation Sensor. Journal of Integrated Circuits and Systems, 2021, 16, 1-6.	0.4	0
13	Study of the UTBB BESOI Tunnel-FET working as a Dual-Technology Transistor. Journal of Integrated Circuits and Systems, 2021, 16, 1-6.	0.4	0
14	Low frequency noise performance of horizontal, stacked and vertical silicon nanowire MOSFETs. Solid-State Electronics, 2021, 184, 108087.	1.4	9
15	Analysis of zero-temperature coefficient behavior on vertically stacked double nanosheet nMOS devices. Microelectronics Journal, 2021, 117, 105277.	2.0	1
16	Gate dielectric material influence on DC behavior of MO(I)SHEMT devices operating up to 150ÂÂ°C. Solid-State Electronics, 2021, 185, 108091.	1.4	4
17	Impact of gate current on the operational transconductance amplifier designed with nanowire TFETs. Solid-State Electronics, 2021, 186, 108099.	1.4	2
18	High Temperature Influence on the Trade-off between gm/I_D and f_T of nanosheet NMOS Transistors with Different Metal Gate Stack. , 2021, , .		0

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19	Experimental Analysis of Trade-Off Between Transistor Efficiency and Unit Gain Frequency of Nanosheet NMOS Transistors. , 2021, , .		0
20	Impact of Gate Dielectric Material on Basic Parameters of MO(I)SHEMT Devices. ECS Transactions, 2020, 97, 53-58.	0.5	1
21	Influence of the Biomaterial Thickness in a Dielectrically Charged Modulated Fringing Field Bio-Tunnel-FET Device. ECS Transactions, 2020, 97, 109-114.	0.5	1
22	Proton-Irradiation Influence on Current Mirror Circuit Using Verilog-A Approach Based on Experimental SOI FinFET Characteristics. ECS Transactions, 2020, 97, 171-177.	0.5	0
23	Intrinsic Voltage Gain of Stacked GAA Nanosheet MOSFETs Operating at High Temperatures. ECS Transactions, 2020, 97, 65-69.	0.5	3
24	Readout Circuit Design Using Experimental Data of Line-TFET Devices. ECS Transactions, 2020, 97, 165-170.	0.5	0
25	Operational transconductance amplifier designed with nanowire tunnel-FET with Si, SiGe and Ge sources using experimental data. Semiconductor Science and Technology, 2020, 35, 095020.	2.0	8
26	Study of Underlapped Finfets Behavior for a Radiation Sensing Purpose. ECS Transactions, 2020, 97, 121-126.	0.5	0
27	Sparse matrices for transient simulations with computing memory reduction. Electric Power Systems Research, 2020, 183, 106266.	3.6	1
28	Analog design with Line-TFET device experimental data: from device to circuit level. Semiconductor Science and Technology, 2020, 35, 055025.	2.0	11
29	Output Conductance of Line-TFETs for Different Device Parameters and its Effect on Basic Analog Circuits. Journal of Integrated Circuits and Systems, 2020, 15, 1-7.	0.4	1
30	Readout Circuit Design Using Experimental Data of Line-TFET Devices. ECS Meeting Abstracts, 2020, MA2020-01, 1390-1390.	0.0	0
31	Proton-Irradiation Influence on Current Mirror Circuit Using Verilog-A Approach Based on Experimental SOI FinFET Characteristics. ECS Meeting Abstracts, 2020, MA2020-01, 1380-1380.	0.0	0
32	Intrinsic Voltage Gain of Stacked GAA Nanosheet MOSFETs Operating at High Temperatures. ECS Meeting Abstracts, 2020, MA2020-01, 1395-1395.	0.0	0
33	Influence of the Biomaterial Thickness in a Dielectrically Charged Modulated Fringing Field Bio-Tunnel-FET Device. ECS Meeting Abstracts, 2020, MA2020-01, 1376-1376.	0.0	1
34	Study of Underlapped Finfets Behavior for a Radiation Sensing Purpose. ECS Meeting Abstracts, 2020, MA2020-01, 1379-1379.	0.0	0
35	Analysis of Omega-Gate Nanowire SOI MOSFET Under Analog Point of View. Journal of Integrated Circuits and Systems, 2020, 15, 1-6.	0.4	0
36	Impact of Gate Dielectric Material on Basic Parameters of MO(I)SHEMT Devices. ECS Meeting Abstracts, 2020, MA2020-01, 1373-1373.	0.0	0

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37	Experimental silicon tunnel-FET device model applied to design a Gm-C filter. Semiconductor Science and Technology, 2020, 35, 095029.	2.0	0
38	Analysis of the Negative-Bias-Temperature-Instability on Omega-Gate Silicon Nanowire SOI MOSFETs with Different Dimensions. Journal of Integrated Circuits and Systems, 2020, 15, 1-5.	0.4	0
39	Optimization of the Dual-Technology Back-Enhanced Field Effect Transistor. , 2020, , .		0
40	AlGaN/GaN MISHEMT analysis from an analog point of view up to 150Â°C. , 2020, , .		0
41	Temperature influence on analog figures-of-merit of nanosheet nMOSFET devices for sub-7nm technology node. , 2020, , .		1
42	Operational Transconductance Amplifier Designed with SiGe-source Nanowire Tunnel-FET using Experimental Lookup Table Model. , 2020, , .		0
43	Comparison between proton irradiated triple gate SOI TFETS and finfets from a TID point of view. Semiconductor Science and Technology, 2019, 34, 065003.	2.0	2
44	Analysis of Omega-Gate Nanowire Devices from Parasitic Conduction to Ionizing Radiation Effects. ECS Journal of Solid State Science and Technology, 2019, 8, Q54-Q60.	1.8	0
45	Performance evaluation of Tunnel-FET basic amplifier circuits. , 2019, , .		9
46	Double Gate Tunnel-FET Working Like a Permittivity Based Biosensor with Different Drain to Gate and Drain to Biomaterial Alignments. ECS Journal of Solid State Science and Technology, 2019, 8, Q50-Q53.	1.8	13
47	Experimental analysis and improvement of the DC method for self-heating estimation. Solid-State Electronics, 2019, 159, 171-176.	1.4	0
48	A Negative-Bias-Temperature-Instability Study on Omega-Gate Silicon Nanowire SOI pMOSFETs. , 2019, , .		1
49	Proposal of a p-type Back-Enhanced Tunnel Field Effect Transistor. , 2019, , .		0
50	Output conductance at saturation like region on Line-TFET for different dimensions. , 2019, , .		2
51	Intrinsic Voltage Gain and Unit-Gain Frequency of Omega-Gate Nanowire SOI MOSFETs. , 2019, , .		2
52	Rebound effect on Charged Based Bio-TFETs for different biomolecules. , 2019, , .		2
53	Transmission Line Model Based on PCB Units and Modified Ï€ Circuits. , 2019, , .		0
54	Device-Based Threading Dislocation Assessment in Germanium Hetero-Epitaxy. , 2019, , .		1

#	Article	IF	Citations
55	Impact of Drain Doping and Biomaterial Thickness in a Dielectrically Modulated Fringing Field Bio-TFET Device. , 2019, , .		0
56	Silicon Nanowire Tunnel-FET Differential Amplifier Using Verilog-A Lookup Table Approach. , 2019, , .		4
57	Comparison between nMOS and pMOS Î©-gate nanowire down to 10 nm width as a function of back gate bias. Semiconductor Science and Technology, 2019, 34, 035003.	2.0	0
58	OTA Performance Comparison Designed with Experimental NW-MOSFET and NW-TFET Devices. , 2019, , .		2
59	Two-stage amplifier design based on experimental Line-Tunnel FET data. , 2019, , .		1
60	Analysis of proton irradiated n- and p-type strained FinFETs at low temperatures down to 100 K. Semiconductor Science and Technology, 2018, 33, 065003.	2.0	2
61	DC method for self-heating estimation applied to FinFET. , 2018, , .		2
62	New approach for removing the self-heating from MOSFET current using only DC characteristics. , 2018, , .		0
63	Ground Plane Impact on the Threshold Voltage of Relaxed Ge pFinFETs. , 2018, , .		0
64	Impact of process and device dimensions on Bio-TFET Sensitivity. , 2018, , .		1
65	Influence of Channel Silicon Thickness and Biological Material Permittivity on nTFET Biosensor. , 2018, , .		1
66	A Tunnel-FET device model based on Verilog-A applied to circuit simulation. , 2018, , .		4
67	Interface Charges Influence on the Subthreshold Region from Triple Gate SOI FinFET to â„¦ -Gate Nanowire Devices. , 2018, , .		2
68	New method for self-heating estimation using only DC measurements. , 2018, , .		1
69	Performance of differential pair circuits designed with line tunnel FET devices at different temperatures. Semiconductor Science and Technology, 2018, 33, 075012.	2.0	5
70	Opposite trends between digital and analog performance for different TFET technologies. , 2018, , .		2
71	Parasitic Conduction on Î©-Gate Nanowires SOI nMOSFETs. ECS Transactions, 2018, 85, 103-109.	0.5	1
72	Impact of Biosensor Permittivity on a Double-Gate nTFET Ambipolar Current. ECS Transactions, 2018, 85, 187-192.	0.5	7

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73	Improvement of gm/IDMethod for Detection of Self-Heating Effects. ECS Transactions, 2018, 85, 73-78.	0.5	0
74	Total ionizing dose influence on proton irradiated triple gate SOI Tunnel FETs. Journal of Integrated Circuits and Systems, 2018, 13, 1-7.	0.4	1
75	Analysis of current mirror circuits designed with line tunnel FET devices at different temperatures. Semiconductor Science and Technology, 2017, 32, 055015.	2.0	6
76	Analysis of the transistor efficiency of gas phase Zn diffusion In<inf>0.53</inf>Ga<inf>0.47</inf>As nTFETs at different temperatures. , 2017, , .		0
77	The Influence of Oxide Thickness and Indium Amount on the Analog Parameters of In_{<italic>x</italic>}Ga_{1â€“<italic>x</italic>}As nTFETs. IEEE Transactions on Electron Devices, 2017, 64, 3595-3600.	3.0	3
78	Experimental comparison between relaxed and strained Ge pFinFETs. , 2017, , .		1
79	Low temperature performance of proton irradiated strained SOI FinFET. , 2017, , .		0
80	Study of line-TFET analog performance comparing with other TFET and MOSFET architectures. Solid-State Electronics, 2017, 128, 43-47.	1.4	29
81	Experimental analysis of differential pairs designed with line tunnel FET devices. , 2017, , .		4
82	Back gate influence on transistor efficiency of SOI nMOS Î©-gate nanowire down to 10nm width. , 2017, , .		1
83	Proton radiation effects on the self-aligned triple gate SOI p-type tunnel FET output characteristic. , 2017, , .		3
84	Simple method for detection of the self-heating signature. , 2017, , .		0
85	Subthreshold region analysis for UTBOX and UTBB SOI nMOSFETs with different channel lengths and silicon thickness. , 2017, , .		0
86	Enhanced model for ZTC in irradiated and strained pFinFET. , 2017, , .		1
87	The influence of low-energy proton irradiaiton on threshold voltage and tranconductance of nanowire SOI n and p-channel transistors. , 2017, , .		0
88	Low temperature influence on long channel STI last process relaxed and strained Ge pFinFETs. , 2017, , .		0
89	Impact of the Zn diffusion process at the source side of In<inf>x</inf>Ga<inf>1â^'x</inf>As nTFETs on the analog parameters down to 10 K. , 2017, , .		0
90	New method for observing self-heating effect using transistor efficiency signature. , 2017, , .		1

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91	Zero Temperature Coefficient behavior for advanced MOSFETs. , 2016, , .		9
92	Back gate bias influence on SOI Î©-gate nanowire down to 10 nm width. , 2016, , .		8
93	(Invited) Generation-Recombination Noise in Advanced CMOS Devices. ECS Transactions, 2016, 75, 111-120.	0.5	2
94	Impact of the low temperature operation on long channel strained Ge pFinFETs fabricated with STI first and last processes. , 2016, , .		2
95	Influence of proton radiation and strain on nFinFET zero temperature coefficient. , 2016, , .		1
96	InGaAs tunnel FET with sub-nanometer EOT and sub-60â€‰mV/dec sub-threshold swing at room temperature. Applied Physics Letters, 2016, 109, .	3.3	48
97	Split CV mobility at low temperature operation of Ge pFinFETs fabricated with STI first and last processes. Semiconductor Science and Technology, 2016, 31, 114002.	2.0	2
98	Analysis of TFET and FinFET differential pairs with active load from 300K to 450K. , 2016, , .		1
99	Low frequency noise and fin width study of silicon passivated germanium pFinFETs. , 2016, , .		1
100	Intrinsic voltage gain of Line-TFETs and comparison with other TFET and MOSFET architectures. , 2016, , .		9
101	Effective hole mobility and low-frequency noise characterization of Ge pFinFETs. , 2016, , .		4
102	Comparative study of vertical GAA TFETs and GAA MOSFETs in function of the inversion coefficient. , 2016, , .		2
103	Influence of the Ge amount at source on transistor efficiency of vertical gate all around TFET for different conduction regimes. , 2016, , .		2
104	Impact of the NW-TFET Diameter on the Efficiency and the Intrinsic Voltage Gain From a Conduction Regime Perspective. IEEE Transactions on Electron Devices, 2016, 63, 2930-2935.	3.0	10
105	Low-Frequency Noise Assessment of Different Ge pFinFET STI Processes. IEEE Transactions on Electron Devices, 2016, 63, 4031-4037.	3.0	8
106	GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes. IEEE Electron Device Letters, 2016, 37, 1092-1095.	3.9	9
107	Analog parameters of solid source Zn diffusion In_XGa_{1â^'X}As nTFETs down to 10 K. Semiconductor Science and Technology, 2016, 31, 124001.	2.0	5
108	Low Temperature Effect on Strained and Relaxed Ge pFinFETs STI Last Processes. ECS Transactions, 2016, 75, 213-218.	0.5	3

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109	Comparative analysis of the intrinsic voltage gain and unit gain frequency between SOI and bulk FinFETs up to high temperatures. Solid-State Electronics, 2016, 123, 124-129.	1.4	7
110	Proton radiation influence on SOI FinFET trade-off between transistor efficiency and unit gain frequency. , 2016, , .		1
111	On the assessment of electrically active defects in high-mobility materials and devices. , 2016, , .		0
112	Low-frequency and random telegraph noise performance of Ge-based and IIIâ€“V devices on a Si platform. , 2016, , .		1
113	Impact of In<inf>x</inf>Ga<inf>1â^'x</inf> composition and source Zn diffusion temperature on intrinsic voltage gain in InGaAs TFETs. , 2016, , .		0
114	Influence of spacer materials on underlapped and self-aligned UTBB SOI nMOSFET. , 2016, , .		0
115	Low-Frequency Noise Analysis and Modeling in Vertical Tunnel FETs With Ge Source. IEEE Transactions on Electron Devices, 2016, 63, 1658-1665.	3.0	69
116	Performance of TFET and FinFET devices applied to current mirrors for different dimensions and temperatures. Semiconductor Science and Technology, 2016, 31, 055001.	2.0	10
117	Analog performance of vertical nanowire TFETs as a function of temperature and transport mechanism. Solid-State Electronics, 2015, 112, 51-55.	1.4	17
118	The Impact of the Ge Concentration in the Source for Vertical Tunnel-FETs. ECS Transactions, 2015, 66, 79-86.	0.5	1
119	High temperature influence on analog parameters of Bulk and SOI nFinFETs. , 2015, , .		1
120	Study of Hysteresis in Vertical Ge-Source Heterojunction Tunnel-FETs at Low Temperature. ECS Transactions, 2015, 66, 179-185.	0.5	0
121	Vertical Nanowire TFET Diameter Influence on Intrinsic Voltage Gain for Different Inversion Conditions. ECS Transactions, 2015, 66, 187-192.	0.5	2
122	Proton Radiation Effects on the Analog Performance of Bulk n- and p-FinFETs. ECS Transactions, 2015, 66, 295-301.	0.5	3
123	Comparison of Current Mirrors Designed with TFET or FinFET Devices for Different Dimensions and Temperatures. ECS Transactions, 2015, 66, 303-308.	0.5	2
124	Impact of Gate Stack Dielectric on Intrinsic Voltage Gain and Low Frequency Noise in Ge pMOSFETs. ECS Transactions, 2015, 66, 309-314.	0.5	1
125	Transconductance hump in vertical gate-all-around tunnel-FETs. , 2015, , .		0
126	Dynamic threshold voltage influence on Ge pMOSFET hysteresis. , 2015, , .		0

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127	Performance comparison between TFET and FinFET differential pair. , 2015, , .		4
128	Impact of diameter on TFET conduction mechanisms. , 2015, , .		1
129	Analysis of analog parameters in NW-TFETs with Si and SiGe source composition at high temperatures. , 2015, , .		5
130	Study of low frequency noise in vertical NW-Tunnel FETs with different source compositions. , 2015, , .		2
131	Comparison between vertical silicon NW-TFET and NW-MOSFETfrom analog point of view. , 2015, , .		4
132	The smaller the noisier? Low frequency noise diagnostics of advanced semiconductor devices. , 2015, , .		2
133	Impact of the diameter of vertical nanowire-tunnel FETs with Si and SiGe source composition on analog parameters. , 2015, , .		3
134	Influence of the Source Composition on the Analog Performance Parameters of Vertical Nanowire-TFETs. IEEE Transactions on Electron Devices, 2015, 62, 16-22.	3.0	29
135	Different stress techniques and their efficiency on triple-gate SOI n-MOSFETs. Solid-State Electronics, 2015, 103, 209-215.	1.4	3
136	Field effect transistors: From mosfet to Tunnel-Fet analog performance perspective. , 2014, , .		5
137	Drain induced barrier thinning on TFETs with different source/drain engineering. , 2014, , .		14
138	(Invited) The Impact of a (Si)Ge Heterojunction on the Analog Performance of Vertical Tunnel FETs. ECS Transactions, 2014, 64, 127-133.	0.5	1
139	Unity gain frequency on FinFET and TFET devices. , 2014, , .		3
140	Comparison of analog performance between SOI and Bulk pFinFET. , 2014, , .		1
141	Graphene for advanced devices applications. , 2014, , .		0
142	Analog performance of standard and uniaxial strained triple-gate SOI FinFETs under x-ray radiation. Semiconductor Science and Technology, 2014, 29, 125015.	2.0	2
143	The effect of X-Ray radiation dose rate on Triple-Gate SOI FinFETs parameters. , 2014, , .		1
144	The effect of X-Ray radiation on DIBL for standard and strained triple-gate SOI MuGFETs. , 2014, , .		0

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145	Threshold voltage extraction in Tunnel FETs. Solid-State Electronics, 2014, 93, 49-55.	1.4	28
146	Fin width influence on analog performance of SOI and bulk FINFETs. , 2014, , .		5
147	Early voltage and intrinsic voltage gain in vertical nanowire-TFETs as a function of temperature. , 2014, , .		0
148	Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature. IEEE Transactions on Electron Devices, 2013, 60, 2493-2497.	3.0	60
149	Comparative study of self-heating effects influence on triple-gate FinFETs fabricated on bulk, SOI and modified substrates. , 2013, , .		3
150	Stress engineering and proton radiation influence on off-state leakage current in triple-gate SOI devices. Solid-State Electronics, 2013, 90, 155-159.	1.4	2
151	Back bias influence on analog performance of pTFET. , 2013, , .		2
152	NW-TFET analog performance for different Ge source compositions. , 2013, , .		11
153	Comparative Experimental Study between Tensile and Compressive Uniaxially Stressed nMuGFETs under X-ray Radiation Focusing on Analog Behavior. ECS Transactions, 2013, 53, 177-185.	0.5	0
154	Fin Dimension Influence on Mechanical Stressors in Triple-Gate SOI nMOSFETs. ECS Transactions, 2013, 53, 187-192.	0.5	0
155	Radiation Influence on Biaxial+Uniaxial Strained Silicon MuGFETs. ECS Transactions, 2013, 50, 205-212.	0.5	0
156	Temperature Influence on Strained nMuGFETs after Proton Radiation. ECS Transactions, 2013, 53, 171-176.	0.5	3
157	Experimental Comparison between pTFET and pFinFET under Analog Operation. ECS Transactions, 2013, 53, 155-160.	0.5	3
158	Influence of X-ray radiation on standard and uniaxial strained triple-gate SOI FinFETs. , 2013, , .		2
159	Radiation effect on standard and strained triple-gate SOI FinFETs parasitic conduction. , 2013, , .		2
160	Biaxial Stress Simulation and Electrical Characterization of Triple-Gate SOI nMOSFETs. ECS Transactions, 2012, 49, 145-152.	0.5	2
161	Temperature Influence on Nanowire Tunnel Field Effect Transistors. ECS Transactions, 2012, 49, 223-230.	0.5	0
162	Uniaxial and/or Biaxial Strain Influence on MuGFET Devices. Journal of the Electrochemical Society, 2012, 159, H570-H574.	2.9	0

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163	Radiation hardness aspects of advanced FinFET and UTBOX devices. , 2012, , .		1
164	Biaxial + uniaxial stress effectiveness in tri-gate SOI nMOSFETs with variable fin dimensions. , 2012, , .		1
165	Experimental analog performance of pTFETs as a function of temperature. , 2012, , .		3
166	Fin width influence on uniaxial stress of triple-gate SOI nMOSFETs. , 2012, , .		2
167	Influence of 60-MeV Proton-Irradiation on Standard and Strained n- and p-Channel MuGFETs. IEEE Transactions on Nuclear Science, 2012, 59, 707-713.	2.0	11
168	Temperature impact on the tunnel fet off-state current components. Solid-State Electronics, 2012, 78, 141-146.	1.4	68
169	Temperature impact on double gate nTFET ambipolar behavior. , 2011, , .		2
170	Impact of proton irradiation on strained triple gate SOI p- and n-MOSFETs. , 2011, , .		3
171	Impact of SEG on uniaxially strained MuGFET performance. Solid-State Electronics, 2011, 59, 13-17.	1.4	2
172	Uniaxial stress efficiency for different fin dimensions of triple-gate SOI nMOSFETs. , 2011, , .		2
173	Strain Effectiveness Dependence on Fin Dimensions and Shape for n-type Triple-Gate MuGFETs. ECS Transactions, 2011, 39, 207-214.	0.5	0
174	A Compact Model and an Extraction Method for the FinFET Spreading Resistance. ECS Transactions, 2011, 39, 255-262.	0.5	2
175	Temperature Influence on Tunnel Field Effect Transistors (TFETs) with Low Ambipolar Currents. ECS Transactions, 2011, 39, 77-84.	0.5	4
176	Global and/or Local Strain Influence on p- and n MuGFET Analog Performance. ECS Transactions, 2011, 35, 145-150.	0.5	0
177	A Simple Electron Mobility Model Considering the Impact of Silicon-Dielectric Interface Orientation for Surrounding Gate Devices. ECS Transactions, 2011, 39, 179-186.	0.5	0
178	Alpha Radiation Incidence Angle Influence on Planar FDSOI nMOSFET. ECS Transactions, 2011, 39, 85-92.	0.5	0
179	Cross-Section Features Influence on Surrounding MuGFETs. ECS Transactions, 2010, 31, 91-98.	0.5	1
180	Fin shape influence on the analog performance of standard and strained MuGFETs. , 2010, , .		8

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181	DIBL performance of 60 MeV proton-irradiated SOI MuGFETs. , 2010, , .		2
182	The "U" Shape Behavior of GIFBE in Function of Back Gate Bias in FinFETs. ECS Transactions, 2009, 19, 317-320.	0.5	0
183	Transconductance ramp effect in high-k triple gate sSOI nFinFETs. , 2009, , .		4
184	Temperature influence on the gate-induced floating body effect parameters in fully depleted SOI nMOSFETs. Solid-State Electronics, 2008, 52, 1751-1754.	1.4	2
185	Analog Performance of Dynamic Threshold Voltage SOI MOSFET.. ECS Transactions, 2008, 14, 169-175.	0.5	1
186	Halo Optimization for 0.13um SOI CMOS Technology. ECS Transactions, 2008, 14, 111-118.	0.5	2
187	The Impact of the Gate Oxide Thickness Reduction on the Gate Induced Floating Body Effect in SOI nMOSFETs. ECS Transactions, 2007, 9, 305-311.	0.5	0
188	The C Shape Behavior of the Floating Body Effect in Function of Temperature in PD SOI nMOSFETs. ECS Transactions, 2007, 6, 107-111.	0.5	0
189	Study of the linear kink effect in PD SOI nMOSFETs. Microelectronics Journal, 2007, 38, 114-119.	2.0	9
190	Impact of the twin-gate structure on the linear kink effect in PD SOI nMOSFETS. Microelectronics Journal, 2006, 37, 681-685.	2.0	5
191	Cryogenic operation of graded-channel silicon-on-insulator nMOSFETs for high performance analog applications. Microelectronics Journal, 2006, 37, 137-144.	2.0	4
192	Electron valence-band tunnelling excess noise in twin-gate silicon-on-insulator MOSFETs. Solid-State Electronics, 2006, 50, 52-57.	1.4	8