Sudeep Pasricha

List of Publications by Year
in descending order

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206	3,350	304368	276539
papers	citations	22 h-index	41 g-index

211	211	211	2014
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Hardware Security in Emerging Photonic Network-on-Chip Architectures. Computer Architecture and Design Methodologies, 2023, , 291-313.	0.5	1
2	Energy and Network Aware Workload Management for Geographically Distributed Data Centers. IEEE Transactions on Sustainable Computing, 2022, 7, 400-413.	2.2	11
3	CHISEL: Compression-Aware High-Accuracy Embedded Indoor Localization With Deep Learning. IEEE Embedded Systems Letters, 2022, 14, 23-26.	1.3	20
4	Silicon Photonic Microring Resonators: A Comprehensive Design-Space Exploration and Optimization Under Fabrication-Process Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3359-3372.	1.9	9
5	TENET: Temporal CNN with Attention for Anomaly Detection in Automotive Cyber-Physical Systems. , 2022, , .		20
6	Interconnects for DNA, Quantum, In-Memory, and Optical Computing: Insights From a Panel Discussion. IEEE Micro, 2022, 42, 40-49.	1.8	11
7	SONIC: A Sparse Neural Network Inference Accelerator with Silicon Photonics for Energy-Efficient Deep Learning. , 2022, , .		7
8	Photonic Networks-on-Chip Employing Multilevel Signaling: A Cross-Layer Comparative Study. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-36.	1.8	0
9	Siamese Neural Encoders for Long-Term Indoor Localization with Mobile Devices. , 2022, , .		10
10	DeFT: A Deadlock-Free and Fault-Tolerant Routing Algorithm for 2.5D Chiplet Networks. , 2022, , .		6
11	Exploiting Process Variations to Secure Photonic NoC Architectures From Snooping Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 850-863.	1.9	9
12	Securing Silicon Photonic NoCs Against Hardware Attacks. , 2021, , 399-421.		0
13	Securing 3D NoCs from Hardware Trojan Attacks. , 2021, , 461-479.		2
14	A Survey on Silicon Photonics for Deep Learning. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-57.	1.8	44
15	BPLight-CNN: A Photonics-Based Backpropagation Accelerator for Deep Learning. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-26.	1.8	9
16	ROBIN: A Robust Optical Binary Neural Network Accelerator. Transactions on Embedded Computing Systems, 2021, 20, 1-24.	2.1	16
17	LATTE: <u>L</u> STM Self- <u>Att</u> ention based Anomaly Detection in <u>E</u> mbedded Automotive Platforms. Transactions on Embedded Computing Systems, 2021, 20, 1-23.	2.1	18
18	ARXON: A Framework for Approximate Communication Over Photonic Networks-on-Chip. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1206-1219.	2.1	6

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19	Dynamic Heuristics for Surveillance Mission Scheduling with Unmanned Aerial Vehicles in Heterogeneous Environments. Transactions on Computational Science and Computational Intelligence, 2021, , 583-605.	0.3	2
20	CrossLight: A Cross-Layer Optimized Silicon Photonic Neural Network Accelerator. , 2021, , .		27
21	Approximate NoC and Memory Controller Architectures for GPGPU Accelerators. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 25-39.	4.0	4
22	SEDAN: Security-Aware Design of Time-Critical Automotive Networks. IEEE Transactions on Vehicular Technology, 2020, 69, 9017-9030.	3.9	19
23	Opportunities for Cross-Layer Design in High-Performance Computing Systems with Integrated Silicon Photonic Networks. , 2020, , .		0
24	INDRA: Intrusion Detection Using Recurrent Autoencoders in Automotive Embedded Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 3698-3710.	1.9	30
25	Variation-Aware Inter-Device Matching in Silicon Photonic Microring Resonator Demultiplexers. , 2020, , .		3
26	A Survey of Resource Management for Processing-In-Memory and Near-Memory Processing Architectures. Journal of Low Power Electronics and Applications, 2020, 10, 30.	1.3	7
27	A Hidden Markov Model based smartphone heterogeneity resilient portable indoor localization framework. Journal of Systems Architecture, 2020, 108, 101806.	2.5	21
28	A Survey of Silicon Photonics for Energy-Efficient Manycore Computing. IEEE Design and Test, 2020, 37, 60-81.	1.1	37
29	Silicon Photonic Microring Resonators: Design Optimization Under Fabrication Non-Uniformity. , 2020, , .		5
30	A Survey on Energy Management for Mobile and IoT Devices. IEEE Design and Test, 2020, 37, 7-24.	1.1	48
31	LORAX: Loss-Aware Approximations for Energy-Efficient Silicon Photonic Networks-on-Chip. , 2020, , .		5
32	SHERPA: A Lightweight Smartphone Heterogeneity Resilient Portable Indoor Localization Framework. , 2019, , .		12
33	SLAM: High Performance and Energy Efficient Hybrid Last Level Cache Architecture for Multicore Embedded Systems. , 2019, , .		2
34	JAMS-SG. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-31.	1.9	9
35	Lightweight Mitigation of Hardware Trojan Attacks in NoC-based Manycore Computing. , 2019, , .		27
36	PortLoc: A Portable Data-Driven Indoor Localization Framework for Smartphones. IEEE Design and Test, 2019, 36, 18-26.	1.1	14

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37	Green Computing with Geo-Distributed Heterogeneous Data Centers. , 2019, , .		0
38	Mobile Network-Aware Middleware Framework for Cloud Offloading: Using Reinforcement Learning to Make Reward-Based Decisions in Smartphone Applications. IEEE Consumer Electronics Magazine, 2019, 8, 42-48.	2.3	7
39	Utility-based resource management in an oversubscribed energy-constrained heterogeneous environment executing parallel applications. Parallel Computing, 2019, 83, 48-72.	1.3	9
40	Overcoming Security Vulnerabilities in Deep Learning--based Indoor Localization Frameworks on Mobile Devices. Transactions on Embedded Computing Systems, 2019, 18, 1-24.	2.1	20
41	DyPhase: A Dynamic Phase Change Memory Architecture With Symmetric Write Latency and Restorable Endurance. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1760-1773.	1.9	13
42	Resilience-Aware Resource Management for Exascale Computing Systems. IEEE Transactions on Sustainable Computing, 2018, 3, 332-345.	2.2	4
43	Minimizing Energy Costs for Geographically Distributed Heterogeneous Data Centers. IEEE Transactions on Sustainable Computing, 2018, 3, 318-331.	2.2	28
44	Overcoming Energy and Reliability Challenges for IoT and Mobile Devices with Data Analytics. , 2018, , .		6
45	Rate-based thermal, power, and co-location aware resource management for heterogeneous data centers. Journal of Parallel and Distributed Computing, 2018, 112, 126-139.	2.7	18
46	HYDRA: Heterodyne Crosstalk Mitigation With Double Microring Resonators and Data Encoding for Photonic NoCs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 168-181.	2.1	20
47	Mixed-criticality scheduling on heterogeneous multicore systems powered by energy harvesting. The Integration VLSI Journal, 2018, 61, 114-124.	1.3	7
48	SOTERIA. , 2018, , .		18
49	PARM. , 2018, , .		2
50	Mitigating the Energy Impacts of VBTI Aging in Photonic Networks-on-Chip Architectures with Multilevel Signaling. , 2018, , .		4
51	Securing Photonic NoC Architectures from Hardware Trojans. , 2018, , .		4
52	DAPPER: Data Aware Approximate NoC for GPGPU Architectures. , 2018, , .		20
53	RAPID: Memory-Aware NoC for Latency Optimized GPGPU Architectures. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 874-887.	2.5	6
54	PARM: Power Supply Noise Aware Resource Management for NoC based Multicore Systems in the Dark Silicon Era. , 2018, , .		4

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55	SOTERIA: Exploiting Process Variations to Enhance Hardware Security with Photonic NoC Architectures. , 2018, , .		2
56	LIBRA: Thermal and Process Variation Aware Reliability Management in Photonic Networks-on-Chip. IEEE Transactions on Multi-Scale Computing Systems, 2018, 4, 758-772.	2.5	26
57	Cross-Layer Thermal Reliability Management in Silicon Photonic Networks-on-Chip. , 2018, , .		3
58	BiGNoC: Accelerating Big Data Computing with Application-Specific Photonic Network-on-Chip Architectures. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 2402-2415.	4.0	17
59	Enabling Prediction for Optimal Fuel Economy Vehicle Control. , 2018, , .		16
60	Advanced Driver-Assistance Systems: A Path Toward Autonomous Vehicles. IEEE Consumer Electronics Magazine, 2018, 7, 18-25.	2.3	332
61	Special session on overcoming reliability and energy-efficiency challenges with silicon photonics for future manycore computing. , 2018, , .		0
62	Adapting Convolutional Neural Networks for Indoor Localization with Smart Mobile Devices. , 2018, , .		49
63	Robust Application Scheduling with Adaptive Parallelism in Dark-Silicon Constrained Multicore Systems. , 2017, , 217-236.		0
64	Islands of heaters: A novel thermal management framework for photonic NoCs. , 2017, , .		14
65	ARTEMIS: An Aging-Aware Runtime Application Mapping Framework for 3D NoC-Based Chip Multiprocessors. IEEE Transactions on Multi-Scale Computing Systems, 2017, 3, 72-85.	2.5	24
66	DELCA. , 2017, , .		0
67	Application of systems theoretic process analysis to a lane keeping assist system. Reliability Engineering and System Safety, 2017, 167, 177-183.	5.1	44
68	DyPhase: A Dynamic Phase Change Memory Architecture with Symmetric Write Latency. , 2017, , .		8
69	Indoor Localization with Smartphones: Harnessing the Sensor Suite in Your Pocket. IEEE Consumer Electronics Magazine, 2017, 6, 70-80.	2.3	43
70	Analyzing voltage bias and temperature induced aging effects in photonic interconnects for manycore computing. , 2017, , .		12
71	SWIFTNoC. ACM Journal on Emerging Technologies in Computing Systems, 2017, 13, 1-27.	1.8	31
72	Improving the Reliability and Energy-Efficiency of High-Bandwidth Photonic NoC Architectures with Multilevel Signaling. , 2017, , .		24

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73	A Runtime Framework for Robust Application Scheduling With Adaptive Parallelism in the Dark-Silicon Era. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 534-546.	2.1	2
74	An Analysis of Resilience Techniques for Exascale Computing Platforms. , 2017, , .		8
75	Optimizing checkpoint intervals for reduced energy use in exascale systems. , 2017, , .		6
76	Data analytics enables energy-efficiency and robustness. , 2017, , .		3
77	Thermal-sensitive design and power optimization for a 3D torus-based optical NoC. , 2017, , .		11
78	JAMS. , 2017, , .		9
79	Uncertainty analysis and propagation for an Auxiliary Power Module. , 2017, , .		6
80	Preemptive resource management for dynamically arriving tasks in an oversubscribed heterogeneous computing system. , 2017, , .		0
81	Energy-efficient and robust middleware prototyping for smart mobile computing. , 2017, , .		4
82	A Software Framework for Rapid Application-Specific Hybrid Photonic Network-on-Chip Synthesis. Electronics (Switzerland), 2016, 5, 21.	1.8	4
83	A Comparative Analysis of Front-End and Back-End Compatible Silicon Photonic On-Chip Interconnects. , 2016, , .		13
84	CHARM: A checkpoint-based resource management framework for reliable multicore computing in the dark silicon era. , 2016, , .		4
85	Enabling green content distribution network by cloud orchestration. , 2016, , .		8
86	PICO. , 2016, , .		21
87	A Performance and Energy Comparison of Fault Tolerance Techniques for Exascale Computing Systems. , 2016, , .		6
88	The Future of NoCs: New Technologies and Architectures. , 2016, , .		0
89	SPECTRA: A Framework for Thermal Reliability Management in Silicon-Photonic Networks-on-Chip. , 2016, , .		16
90	Dynamic Resource Management for Parallel Tasks in an Oversubscribed Energy-Constrained Heterogeneous Environment. , 2016, , .		5

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91	Run-time laser power management in photonic NoCs with on-chip semiconductor optical amplifiers. , 2016, , .		14
92	Mitigation of homodyne crosstalk noise in silicon photonic NoC architectures with tunable decoupling. , 2016, , .		16
93	Online Resource Management in Thermal and Energy Constrained Heterogeneous High Performance Computing. , 2016, , .		3
94	HPC node performance and energy modeling with the co-location of applications. Journal of Supercomputing, 2016, 72, 4771-4809.	2.4	13
95	Process variation aware crosstalk mitigation for DWDM based photonic NoC architectures. , 2016, , .		10
96	Memory-aware circuit overlay NoCs for latency optimized GPGPU architectures. , 2016, , .		2
97	Massed Refresh: An Energy-Efficient Technique to Reduce Refresh Overhead in Hybrid Memory Cube Architectures. , 2016, , .		9
98	A System-Level Cosynthesis Framework for Power Delivery and On-Chip Data Networks in Application-Specific 3-D ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3-16.	2.1	9
99	VARSHA: Variation and Reliability-Aware Application Scheduling with Adaptive Parallelism in the Dark-Silicon Era. , 2015, , .		12
100	Energy cost optimization for geographically distributed heterogeneous data centers. , 2015, , .		8
101	Crosstalk Mitigation for High-Radix and Low-Diameter Photonic NoC Architectures. IEEE Design and Test, 2015, 32, 29-39.	1.1	32
102	A Methodology for Co-Location Aware Application Performance Modeling in Multicore Computing. , 2015, , .		10
103	Improving crosstalk resilience with wavelength spacing in photonic crossbar-based network-on-chip architectures. , 2015, , .		15
104	ARTEMIS. , 2015, , .		3
105	Integrated photonics in future multicore computing. , 2015, , .		0
106	3D-ProWiz: An Energy-Efficient and Optically-Interfaced 3D DRAM Architecture with Reduced Data Access Overhead. IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 168-184.	2.5	13
107	3-D WiRED: A Novel WIDE I/O DRAM With Energy-Efficient 3-D Bank Organization. IEEE Design and Test, 2015, 32, 71-80.	1.1	6
108	A novel 3D graphics DRAM architecture for high-performance and low-energy memory accesses. , 2015, , .		3

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109	Soft and Hard Reliability-Aware Scheduling for Multicore Embedded Systems with Energy Harvesting. IEEE Transactions on Multi-Scale Computing Systems, 2015, 1, 220-235.	2.5	11
110	LearnLoc: A framework for smart indoor localization with embedded mobile devices. , 2015, , .		28
111	A middleware framework for application-aware and user-specific energy optimization in smart mobile devices. Pervasive and Mobile Computing, 2015, 20, 47-63.	2.1	22
112	Reconfigurable Silicon-Photonic Network with Improved Channel Sharing for Multicore Architectures. , 2015, , .		17
113	Makespan and Energy Robust Stochastic Static Resource Allocation of a Bag-of-Tasks to a Heterogeneous Computing System. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 2791-2805.	4.0	19
114	Utility maximizing dynamic resource management in an oversubscribed energy-constrained heterogeneous computing system. Sustainable Computing: Informatics and Systems, 2015, 5, 14-30.	1.6	31
115	Run-Time Management for Multicore Embedded Systems With Energy Harvesting. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2876-2889.	2.1	17
116	Process variation aware dynamic power management in multicore systems with extended range voltage/frequency scaling. , 2015, , .		9
117	Power and Thermal-Aware Workload Allocation in Heterogeneous Data Centers. IEEE Transactions on Computers, 2015, 64, 477-491.	2.4	49
118	PRATHAM: A power delivery-aware and thermal-aware mapping framework for parallel embedded applications on 3D MPSoCs. , 2014, , .		0
119	3D-Wiz: A novel high bandwidth, optically interfaced 3D DRAM architecture with reduced random access time. , 2014, , .		14
120	Energy-aware resource management for computing systems. , 2014, , .		3
121	METEOR. Transactions on Embedded Computing Systems, 2014, 13, 1-33.	2.1	47
122	Utility Driven Dynamic Resource Management in an Oversubscribed Energy-Constrained Heterogeneous System. , 2014, , .		5
123	HEFT. , 2014, , .		5
124	Secure cross-platform hybrid mobile enterprise voice agent. , 2014, , .		1
125	A hybrid framework for application allocation and scheduling in multicore systems with energy harvesting. , 2014, , .		7
126	HELIX: Design and synthesis of hybrid nanophotonic application-specific network-on-chip architectures. , 2014, , .		8

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127	Fault-aware application scheduling in low-power embedded systems with energy harvesting. , 2014, , .		7
128	Process Variation Aware Synthesis of Application-Specific MPSoCs to Maximize Yield. , 2014, , .		4
129	Guest Editors' Introduction: Silicon Nanophotonics for Future Multicore Architectures. IEEE Design and Test, 2014, 31, 6-8.	1.1	1
130	NoC Scheduling for Improved Application-Aware and Memory-Aware Transfers in Multi-core Systems. , 2014, , .		11
131	An application-aware heterogeneous prioritization framework for NoC based chip multiprocessors. , 2014, , .		8
132	Silicon Nanophotonics for Future Multicore Architectures: Opportunities and Challenges. IEEE Design and Test, 2014, 31, 9-17.	1.1	11
133	Context-Aware Energy Enhancements for Smart Mobile Devices. IEEE Transactions on Mobile Computing, 2014, 13, 1720-1732.	3.9	51
134	Thermal, power, and co-location aware resource allocation in heterogeneous high performance computing systems. , 2014, , .		1
135	Energy and Deadline Constrained Robust Stochastic Static Resource Allocation. Lecture Notes in Computer Science, 2014, , 761-771.	1.0	2
136	Thermal-aware semi-dynamic power management for multicore systems with energy harvesting. , 2013, , .		4
137	Reliability-aware and energy-efficient synthesis of NoC based MPSoCs. , 2013, , .		1
138	VERVE: A framework for variation-aware energy efficient synthesis of NoC-based MPSoCs with voltage islands. , 2013, , .		9
139	Deadline and energy constrained dynamic resource allocation in a heterogeneous computing environment. Journal of Supercomputing, 2013, 63, 326-347.	2.4	21
140	On-Chip Optical Ring Bus Communication Architecture for Heterogeneous MPSoC. Embedded Systems, 2013, , 153-176.	0.6	0
141	MultiMaKe. Transactions on Embedded Computing Systems, 2013, 12, 1-25.	2.1	2
142	Harvesting-aware energy management for multicore platforms with hybrid energy storage. , 2013, , .		6
143	Exploiting spatiotemporal and device contexts for energy-efficient mobile embedded systems. , 2012, , .		15
144	A Power Delivery Network Aware Framework for Synthesis of 3D Networks-on-Chip with Multiple Voltage Islands. , 2012, , .		8

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145	Thermal-Aware Performance Optimization in Power Constrained Heterogenous Data Centers. , 2012, , .		4
146	Characterizing Vulnerability of Network Interfaces in Embedded Chip Multiprocessors. IEEE Embedded Systems Letters, 2012, 4, 41-44.	1.3	4
147	A Particle Swarm Optimization approach for synthesizing application-specific hybrid photonic networks-on-chip. , 2012, , .		14
148	A framework for low power synthesis of interconnection networks-on-chip with multiple voltage islands. The Integration VLSI Journal, 2012, 45, 271-281.	1.3	8
149	OPAL: A multi-layer hybrid photonic NoC for 3D ICs. , 2011, , .		30
150	Analysis of on-chip interconnection network interface reliability in multicore systems. , 2011, , .		2
151	POSEIDON: A framework for application-specific Network-on-Chip synthesis for heterogeneous chip multiprocessors. , 2011, , .		13
152	A low overhead fault tolerant routing scheme for 3D Networks-on-Chip. , 2011, , .		57
153	A Multi-Granularity Power Modeling Methodology for Embedded Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 668-681.	2.1	31
154	Energy-Constrained Dynamic Resource Allocation in a Heterogeneous Computing Environment. , 2011, , .		4
155	Stochastically robust static resource allocation for energy minimization with a makespan constraint in a heterogeneous computing environment. , 2011, , .		7
156	AURA: An application and user interaction aware middleware framework for energy optimization in mobile devices. , 2011, , .		23
157	NS-FTR: A fault tolerant routing scheme for networks on chip with permanent and runtime intermittent faults. , 2011, , .		17
158	OE+IOE. , 2010, , .		20
159	CAPPS: A Framework for Powerâ€“Performance Tradeoffs in Bus-Matrix-Based On-Chip Communication Architecture Synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 209-221.	2.1	9
160	Evaluating Carbon Nanotube Global Interconnects for Chip Multiprocessor Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1376-1380.	2.1	13
161	NARCO: Neighbor Aware Turn Model-Based Fault Tolerant Routing for NoCs. IEEE Embedded Systems Letters, 2010, 2, 85-89.	1.3	16
162	UC-PHOTON: A novel hybrid photonic network-on-chip for multiple use-case applications. , 2010, , .		13

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163	Inter-kernel data reuse and pipelining on chip-multiprocessors for multimedia applications. , 2009, , .		5
164	Exploring serial vertical interconnects for 3D ICs. , 2009, , .		87
165	Exploring hybrid photonic networks-on-chip foremerging chip multiprocessors. , 2009, , .		25
166	System-level PVT variation-aware power exploration of on-chip communication architectures. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-25.	1.9	3
167	Exploring Carbon Nanotube Bundle Global Interconnects for Chip Multiprocessor Applications. , 2009, , .		5
168	Cross-Abstraction Functional Verification and Performance Analysis of Chip Multiprocessor Designs. IEEE Transactions on Industrial Informatics, 2009, 5, 241-256.	7.2	4
169	Dynamically reconfigurable on-chip communication architectures for multi use-case chip multiprocessor applications. , 2009, , .		5
170	A Methodology for Power-aware Pipelining via High-Level Performance Model Evaluations. , 2009, , .		4
171	On chip Communication-Architecture Based Thermal Management for SoCs. , 2009, , .		3
172	Adaptive Scratch Pad Memory Management for Dynamic Behavior of Multimedia Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 554-567.	1.9	24
173	System level performance analysis of carbon nanotube global interconnects for emerging chip multiprocessors. , 2008, , .		6
174	Incorporating PVT Variations in System-Level Power Exploration of On-Chip Communication Architectures. , 2008, , .		5
175	ORB: An on-chip optical ring bus communication architecture for multi-processor systems-on-chip. , 2008, , .		33
176	Dynamic register file resizing and frequency scaling to improve embedded processor performance and energy-delay efficiency. , 2008, , .		10
177	Fast exploration of bus-based communication architectures at the CCATB abstraction. Transactions on Embedded Computing Systems, 2008, 7, 1-32.	2.1	311
178	A framework for memory-aware multimedia application mapping on chip-multiprocessors. , 2008, , .		5
179	Trends in Emerging On-Chip Interconnect Technologies. IPSJ Transactions on System LSI Design Methodology, 2008, 1, 2-17.	0.5	30
180	On-Chip Communication Architecture Standards. , 2008, , 43-100.		2

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181	Synthesis of On-Chip Communication Architectures. , 2008, , 185-252.		20
182	Encoding Techniques for On-Chip Communication Architectures. , 2008, , 253-300.		7
183	Networks-On-Chip. , 2008, , 439-471.		6
184	Compiler driven data layout optimization for regular/irregular array access patterns. , 2008, , .		11
185	Compiler driven data layout optimization for regular/irregular array access patterns. ACM SIGPLAN Notices, 2008, 43, 41-50.	0.2	1
186	On-Chip Communication Architecture Refinement and Interface Synthesis. , 2008, , 341-366.		0
187	Custom Bus-Based On-Chip Communication Architecture Design. , 2008, , 301-340.		1
188	Models for Power and Thermal Estimation. , 2008, , 143-184.		0
189	Basic Concepts of Bus-Based Communication Architectures. , 2008, , 17-41.		1
190	Models for Performance Exploration. , 2008, , 101-142.		0
191	Verification and Security Issues in On-Chip Communication Architecture Design. , 2008, , 367-402.		0
192	Emerging On-Chip Interconnect Technologies. , 2008, , 473-507.		1
193	Improving performance and reducing energy-delay with adaptive resource resizing for out-of-order embedded processors. ACM SIGPLAN Notices, 2008, 43, 71-78.	0.2	3
194	A Framework for Cosynthesis of Memory and Communication Architectures for MPSoC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 408-420.	1.9	20
195	BMSYN: Bus Matrix Communication Architecture Synthesis for MPSoC. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1454-1464.	1.9	23
196	System level power estimation methodology with H.264 decoder prediction IP case study. , 2007, , .		10
197	Enabling heterogeneous cycle-based and event-driven simulation in a design flow integrated using the SPIRIT consortium specifications. Design Automation for Embedded Systems, 2007, 11, 119-140.	0.7	3
198	Formal performance evaluation of AMBA-based system-on-chip designs. , 2006, , .		12

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199	Constraint-driven bus matrix synthesis for MPSoC. , 2006, , .		28
200	System-level power-performance trade-offs in bus matrix communication architecture synthesis. , 2006, , .		31
201	Floorplan-aware automated synthesis of bus-based communication architectures. , 2005, , .		50
202	Automated throughput-driven synthesis of bus-based communication architectures. , 2005, , .		6
203	Extending the transaction level modeling approach for fast communication architecture exploration. , 2004, , .		61
204	Fast exploration of bus-based on-chip communication architectures. , 2004, , .		55
205	Dynamic backlight adaptation for low-power handheld devices. IEEE Design and Test of Computers, 2004, 21, 398-405.	1.4	41
206	Toward Improving Vehicle Fuel Economy with ADAS. SAE International Journal of Connected and Automated Vehicles, 0, 1, 81-92.	0.4	19