Wei-Chung Hsu

List of Publications by Year
in descending order

70	688	1163117 8	1125743 13
papers	citations	h-index	g-index

71	71	71	316
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	HQEMU. , 2012, , .		84
2	Dynamic Helper Threaded Prefetching on the Sun UltraSPARC CMP Processor. , 0, , .		59
3	On the Minimization of Loads/Stores in Local Register Allocation. IEEE Transactions on Software Engineering, 1989, 15, 1252-1260.	5.6	43
4	Exploring speculative parallelism in SPEC2006. , 2009, , .		31
5	PQEMU: A Parallel System Emulator Based on QEMU. , 2011, , .		29
6	LLBT. , 2012, , .		27
7	Dynamic performance tuning for speculative threads. , 2009, , .		26
8	Data Dependence Profiling for Speculative Optimizations. Lecture Notes in Computer Science, 2004, , 57-72.	1.3	25
9	A performance study of instruction cache prefetching methods. IEEE Transactions on Computers, 1998, 47, 497-508.	3.4	20
10	A Retargetable Static Binary Translator for the ARM Architecture. Transactions on Architecture and Code Optimization, 2014, 11, 1-25.	2.0	20
11	Energy efficient speculative threads. , 2010, , .		18
12	A method-based ahead-of-time compiler for android applications. , 2011, , .		17
13	Efficient memory virtualization for Cross-ISA system mode emulation. , 2014, , .		15
14	A General Compiler Framework for Speculative Optimizations Using Data Speculative Code Motion. , 0, , .		14
15	ReRanz. , 2017, , .		14
16	LnQ: Building High Performance Dynamic Binary Translators with Existing Compiler Backends. , 2011, , .		13
17	An LLVM-based hybrid binary translation system. , 2012, , .		13
18	DBILL. , 2014, , .		13

#	Article	IF	Citations
19	Exploiting SIMD Asymmetry in ARM-to-x86 Dynamic Binary Translation. Transactions on Architecture and Code Optimization, 2019, 16, 1-24.	2.0	13
20	A compiler framework for speculative optimizations. Transactions on Architecture and Code Optimization, 2004, 1, 247-271.	2.0	12
21	Improving dynamic binary optimization through early-exit guided code region formation. , 2013, , .		11
22	Building a KVM-based Hypervisor for a Heterogeneous System Architecture Compliant System. , 2016, , .		11
23	Improving SIMD Parallelism via Dynamic Binary Translation. Transactions on Embedded Computing Systems, 2018, 17, 1-27.	2.9	11
24	Dynamic trace selection using performance monitoring hardware sampling. , 0, , .		9
25	COBRA: An Adaptive Runtime Binary Optimization Framework for Multithreaded Applications. Parallel Processing (ICPP), Proceedings of the International Symposium, 2007, , .	0.0	7
26	HSPT. , 2015, , .		7
27	Exploiting Longer SIMD Lanes in Dynamic Binary Translation. , 2016, , .		7
28	Performance of Runtime Optimization on BLAST. , 0, , .		6
29	Effective code discovery for ARM/Thumb mixed ISA binaries in a static binary translator. , 2013, , .		6
30	HSAemu. , 2014, , .		6
31	Efficient and Retargetable Dynamic Binary Translation on Multicores. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 622-632.	5.6	6
32	A dynamic binary translation system in a client/server environment. Journal of Systems Architecture, 2015, 61, 307-319.	4.3	6
33	Exploiting Asymmetric SIMD Register Configurations in ARM-to-x86 Dynamic Binary Translation. , 2017, , .		6
34	SIMD Code Translation in an Enhanced HQEMU. , 2015, , .		5
35	Runtime techniques for efficient Ray-Tracing on heterogeneous systems. , 2015, , .		5
36	Efficient and retargetable SIMD translation in a dynamic binary translator. Software - Practice and Experience, 2018, 48, 1312-1330.	3.6	5

#	Article	IF	Citations
37	Improving SIMD Code Generation in QEMU. , 2015, , .		5
38	The design and implementation of heterogeneous multicore systems for energy-efficient speculative thread execution. Transactions on Architecture and Code Optimization, 2013, 10, 1-29.	2.0	4
39	Automatic validation for binary translation. Computer Languages, Systems and Structures, 2015, 43, 96-115.	1.4	4
40	A pipeline-based runtime technique for improving Ray-Tracing on HSA-compliant systems. , 2016, , .		4
41	Speculative register promotion using advanced load address table (ALAT). , 0, , .		3
42	Region Monitoring for Local Phase Detection in Dynamic Optimization Systems. , 0, , .		3
43	An Evaluation of Misaligned Data Access Handling Mechanisms in Dynamic Binary Translation Systems. , 2009, , .		3
44	A hybrid just-in-time compiler for android. , 2012, , .		3
45	On Static Binary Translation of ARM/Thumb Mixed ISA Binaries. Transactions on Embedded Computing Systems, 2017, 16, 1-25.	2.9	3
46	ReRanz. ACM SIGPLAN Notices, 2017, 52, 143-156.	0.2	3
47	Exploring hidden coherency of Ray-Tracing for heterogeneous systems using online feedback methodology. Visual Computer, 2018, 34, 633-643.	3.5	3
48	HSPT. ACM SIGPLAN Notices, 2015, 50, 53-64.	0.2	3
49	Performance characterization of data mining benchmarks. , 2010, , .		3
50	EFFECTIVENESS OF COMPILER-DIRECTED PREFETCHING ON DATA MINING BENCHMARKS. Journal of Circuits, Systems and Computers, 2012, 21, 1240006.	1.5	2
51	An Adaptive Heterogeneous Runtime Framework for Irregular Applications. Journal of Signal Processing Systems, 2015, 80, 245-259.	2.1	2
52	Efficient Synthetic Light Field Rendering on Heterogeneous Systems Using a Pipeline-Based Runtime Design. , 2017, , .		2
53	Optimizing Control Transfer and Memory Virtualization in Full System Emulators. Transactions on Architecture and Code Optimization, 2016, 12, 1-24.	2.0	2
54	On the impact of naming methods for heap-oriented pointers in C programs. , 0, , .		1

#	Article	IF	Citations
55	Analysis of Statistical Sampling in Microarchitecture Simulation: Metric, Methodology and Program Characterization. , 2007, , .		1
56	Dynamic register promotion of stack variables. , 2011, , .		1
57	Improving dynamic binary optimization through early-exit guided code region formation. ACM SIGPLAN Notices, 2013, 48, 23-32.	0.2	1
58	Dynamic and Adaptive Calling Context Encoding. , 2014, , .		1
59	Processor-Tracing Guided Region Formation in Dynamic Binary Translation. Transactions on Architecture and Code Optimization, 2019, 15, 1-25.	2.0	1
60	The use of intermediate memories for low-latency memory access in supercomputer scalar units. Journal of Supercomputing, 1990, 4, 5-21.	3.6	0
61	Toward Effective Scalar Hardware for Highly Vectorizable Applications. Journal of Parallel and Distributed Computing, 1993, 19, 147-162.	4.1	0
62	The performance of runtime data cache prefetching in a dynamic optimization system. , 0, , .		0
63	Reducing Code Size by Graph Coloring Register Allocation and Assignment Algorithm for Mixed-Width ISA Processor. , 2009, , .		0
64	Dynamic performance tuning for speculative threads. Computer Architecture News, 2009, 37, 462-473.	2.5	0
65	Efficient and effective misaligned data access handling in a dynamic binary translation system. Transactions on Architecture and Code Optimization, 2011, 8, 1-29.	2.0	0
66	Extended Instruction Exploration for Multiple-Issue Architectures. Transactions on Embedded Computing Systems, 2014, 13, 1-28.	2.9	0
67	HSAemu 2.0. , 2016, , .		0
68	A pipeline-based heterogeneous framework for efficient synthetic light field rendering. ACM SIGAPP Applied Computing Review: A Publication of the Special Interest Group on Applied Computing, 2018, 18, 19-29.	0.9	0
69	Automatically Migrating Sequential Applications to Heterogeneous System Architecture. , 2018, , .		0
70	An Adaptive Heterogeneous Runtime for Irregular Applications in the Case of Ray-Tracing (Extended) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 5	1.3	0