Pradeep Kumar

List of Publications by Year
in descending order

52	167	1684188 5	1474206 9
papers	citations	h-index	g-index

52	52	52	105
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Wide-band resistorless all-pass sections with single element tuning. International Journal of Electronics, 2007, 94, 597-604.	1.4	28
2	Analysis and comparison of leakage power reduction techniques in CMOS circuits. , 2015, , .		17
3	DVCC-Based Single Element Frequenz 61 (2007) 5-6 Controlled Oscillators Using All-Grounded Components and Simultaneous Current-Voltage Mode Outputs. Frequenz, 2007, 61, .	0.9	13
4	16 Bit Power Efficient Carry Select Adder. , 2019, , .		11
5	RGB image steganography on multiple frame video using LSB technique. , 2015, , .		9
6	Variable Q all-pass, notch and band-pass filters using single CCII. Frequenz, 2005, 59, .	0.9	7
7	Effect of Surface Passivation on the Electrical Characteristics of Nanoscale AlGaN/GaN HEMT. IOP Conference Series: Materials Science and Engineering, 2017, 225, 012095.	0.6	6
8	Analysis of multilayered SAW based gas sensor. , 2017, , .		5
9	A boosted negative bit-line SRAM with write-assisted cell in 45 nm CMOS technology. Journal of Semiconductors, 2018, 39, 025001.	3.7	5
10	Design and analysis of high performance and low power FFT for DSP datapath using Vedic Multipliers. International Journal of Electronics Letters, 2022, 10, 188-199.	1.2	5
11	Performance analysis of different PN sequence and Orthogonal Spreading sequences in DS-SS. , 2014, , .		4
12	Neural Network based indicative ECG classification. , 2014, , .		4
13	Performance analysis of least mean square algorithm for different step size parameters with different filter order and iterations. , 2015, , .		4
14	An efficient multistage security system for user authentication. , 2016, , .		4
15	Low power and temperature compatible FinFET based full adder circuit with optimised area. , 2016, , .		4
16	FFT using Power Efficient Vedic Multiplier. International Journal of Innovative Technology and Exploring Engineering, 2019, 8, 603-608.	0.3	4
17	Power efficient, clock gated multiplexer based full adder cell using 28 nm technology. AIP Conference Proceedings, 2016, , .	0.4	3
18	Noise Reduction from ECG Signal Using Error Normalized Step Size Least Mean Square Algorithm (ENSS) with Wavelet Transform. Advances in Intelligent Systems and Computing, 2019, , 163-171.	0.6	3

#	Article	IF	Citations
19	Optimization of Adaptive Noise Canceller with Grey Wolf Optimizer for EEG/ERP Signal Noise Cancellation. , 2019, , .		3
20	A Survey with Emphasis on Adaptive filter, Structure, LMS and NLMS Adaptive Algorithm for Adaptive Noise Cancellation System. Journal of Engineering Science and Technology Review, 2017, 10, 150-160.	0.4	3
21	On adaptive HVAC based on a De-Centralized algorithm using K:1 transmission protocol for Autonomous Wireless Sensor Network. , 2010, , .		2
22	An approach to implement LMS and NLMS adaptive noise cancellation algorithm in frequency domain. , 2014, , .		2
23	Analysis and implementation of ripple and area efficient charge pump circuits. , 2015, , .		2
24	Physical design implementation of 32-bit AMBA ASB APB module with improved performance. , 2016, , .		2
25	Fast integral image computing scheme for vision based applications. , 2017, , .		2
26	High Input Impendance Biquadratic Filter Using Three Translinear Current Conveyors and Ground Capacitors. , 2018, , .		2
27	Enhanced AES Architecture using Extended Set ALU at 28nm FPGA. , 2018, , .		2
28	A User Programmable Electro-optic Device for Testing Laser Seekers. Defence Science Journal, 2014, 64, 88-92.	0.8	2
29	Power and Area Efficient Vedic Multipliers Using Modified CSLA Architectures for DSP. Journal of Advanced Research in Dynamical and Control Systems, 2019, 11, 44-51.	0.2	2
30	Design and implementation of MAC unit based on Vedic Square, and its application. , 2015, , .		1
31	An approach to implement VSS-LMS algorithm in frequency domain for adaptive noise cancellation. , 2015, , .		1
32	Design and implementation of low power clock gated 64-bit ALU on ultra scale FPGA. AIP Conference Proceedings, 2016, , .	0.4	1
33	Multiphysics simulation of InP NWT for high speed digital applications. , 2017, , .		1
34	A dual V t disturb-free subthreshold SRAM with write-assist and read isolation. Journal of Semiconductors, 2018, 39, 025002.	3.7	1
35	Delay Efficient Vedic Multiplier for DSP. International Journal of Innovative Technology and Exploring Engineering, 2019, 8, 499-501.	0.3	1
36	Intelligent Multilevel Car Parking System Using RFID. International Journal of Simulation: Systems, Science and Technology, 0, , .	0.0	1

#	Article	IF	Citations
37	A high Q band pass filter using translinear current conveyor and unity gain buffer. , 0, , .		0
38	An efficient MAC unit with low area consumption. , 2015, , .		0
39	OIV-CMOS: A novel approach towards leakage power reduction. , 2015, , .		0
40	Effect of substrate material on sensing behaviour of SAW based gas sensors. AIP Conference Proceedings, 2017, , .	0.4	0
41	Analysis of schottky barrier indium arsenide nanowire MOSFET for high frequency application. , 2017, , .		0
42	Thermal analysis of III-V transistor at high frequencies. , 2017, , .		0
43	HDL implementation of high performance 16 bit processor on FPGA. , 2017, , .		0
44	Simulation of Self-Heating Effect for Different Gate Lengths and its Influence on DC Characteristics of AlGaN/GaN HEMT. , 2018, , .		0
45	Implementation of Normalized Data Non-Linearity and Constraint Stability Least Mean Square algorithm with a new SuFee model for Adaptive Noise Cancellation. , 2018, , .		0
46	AN OPTIMAL APPROACH FOR EEG/ERP NOISE CANCELLATION USING ADAPTIVE FILTER WITH OPPOSITIONAL WHALE OPTIMIZATION ALGORITHM. Biomedical Engineering - Applications, Basis and Communications, 2019, 31, 1950035.	0.6	0
47	Wireless Power Transfer to Low Power Devices. , 2019, , .		0
48	A Hybrid Optimization Method OWGWA for EEG/ERP Adaptive Noise Canceller With Controlled Search Space. International Journal of Swarm Intelligence Research, 2020, 11, 30-48.	0.7	0
49	DESIGNING DUAL PORT RAM FOR TESTABILITY. Far East Journal of Electronics and Communications, 0, , 667-676.	0.2	0
50	Optimal C code Implementation of OWGWA-CSS Algorithm on TMS320C6713 DSK. International Journal of Innovative Technology and Exploring Engineering, 2019, 8, 2515-2520.	0.3	0
51	Simulation Analysis of Wireless Power Transfer for Future Office Communication Systems. International Journal of Innovative Technology and Exploring Engineering, 2019, 8, 533-538.	0.3	0
52	Analysis of SRAM bit cell topologies in submicron CMOS technology. International Journal of Simulation: Systems, Science and Technology, 0, , .	0.0	0