

Marif Daula Siddique

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

61
papers

889
citations

14
h-index

27
g-index

68
ext. papers

1,482
ext. citations

2.8
avg, IF

5.35
L-index

#	Paper	IF	Citations
61	Compact Quadratic Boost Switched-Capacitor Inverter. <i>IEEE Transactions on Industry Applications</i> , 2022 , 1-1	4.3	0
60	A 9 and 13-Level Switched-Capacitor-Based Multilevel Inverter with enhanced Self-Balanced Capacitor Voltage Capability. <i>IEEE Journal of Emerging and Selected Topics in Power Electronics</i> , 2022 , 1-1	5.6	3
59	Single-Phase Boost Switched-Capacitor Based Multilevel Inverter Topology with Reduced Switching Devices. <i>IEEE Journal of Emerging and Selected Topics in Power Electronics</i> , 2021 , 1-1	5.6	6
58	A New Configuration of Nine-Level Boost Inverter with Reduced Component Count. <i>E-Prime</i> , 2021 , 1, 100010		0
57	Experimental validation of nine-level switched-capacitor inverter topology with high voltage gain. <i>International Journal of Circuit Theory and Applications</i> , 2021 , 49, 2479	2	3
56	Experimental validation of new self-voltage balanced 9L-ANPC inverter for photovoltaic applications. <i>Scientific Reports</i> , 2021 , 11, 5067	4.9	5
55	A transformerless high gain dc/dc boost converter with reduced voltage stress. <i>International Transactions on Electrical Energy Systems</i> , 2021 , 31, e12877	2.2	9
54	An improved asymmetrical multi-level inverter topology with boosted output voltage and reduced components count. <i>IET Power Electronics</i> , 2021 , 14, 2052-2066	2.2	4
53	A twice boost nine-level switched-capacitor multilevel (2B-9L-SCMLI) inverter with self-voltage balancing capability. <i>International Journal of Circuit Theory and Applications</i> , 2021 , 49, 2578	2	3
52	A new family of boost active neutral point clamped inverter topology with reduced switch count. <i>IET Power Electronics</i> , 2021 , 14, 1433-1443	2.2	2
51	A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources. <i>International Journal of Electrical Power and Energy Systems</i> , 2021 , 128, 106730	5.1	10
50	Quadruple Boost Multilevel Inverter (QB-MLI) Topology With Reduced Switch Count. <i>IEEE Transactions on Power Electronics</i> , 2021 , 36, 7372-7377	7.2	15
49	Single-Phase Step-Up Switched-Capacitor-Based Multilevel Inverter Topology With SHEPWM. <i>IEEE Transactions on Industry Applications</i> , 2021 , 57, 3107-3119	4.3	42
48	Compact Seven-Level Boost Type Inverter Topology. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2021 , 68, 1358-1362	3.5	11
47	Implementation and Analysis of a 15-Level Inverter Topology With Reduced Switch Count. <i>IEEE Access</i> , 2021 , 9, 40623-40634	3.5	6
46	A New Family of Step-Up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies With Dual Input Voltage Sources. <i>IEEE Access</i> , 2021 , 9, 4398-4410	3.5	13
45	A Cross Connected Asymmetrical Switched-Capacitor Multilevel Inverter. <i>IEEE Access</i> , 2021 , 9, 96416-96429	3.5	5

44	An Improved 15-Level Asymmetrical Multilevel Inverter with Reduced Switch Count. <i>Lecture Notes in Electrical Engineering</i> , 2021 , 709-718	0.2	0
43	Recent trends and review on switched-capacitor-based single-stage boost multilevel inverter. <i>International Transactions on Electrical Energy Systems</i> , 2021 , 31, e12730	2.2	12
42	Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count. <i>International Journal of Circuit Theory and Applications</i> , 2021 , 49, 1757-1775	2	6
41	A New Multilevel Inverter Topology with Reduced DC Sources. <i>Energies</i> , 2021 , 14, 4709	3.1	5
40	Asynchronous Particle Swarm Optimization-Genetic Algorithm (APSO-GA) based Selective Harmonic Elimination in a Cascaded H-Bridge Multilevel Inverter. <i>IEEE Transactions on Industrial Electronics</i> , 2021 , 1-1	8.9	30
39	Dual asymmetrical dc voltage source based switched capacitor boost multilevel inverter topology. <i>IET Power Electronics</i> , 2020 , 13, 1481-1486	2.2	23
38	Dual input switched-capacitor-based single-phase hybrid boost multilevel inverter topology with reduced number of components. <i>IET Power Electronics</i> , 2020 , 13, 881-891	2.2	31
37	New Switched-Capacitor based Boost Seven-Level ANPC (7L-ANPC) Boost Inverter Topology 2020 ,		2
36	Switched-Capacitor Based Seven-Level Triple Voltage Gain Boost Inverter (7L-TVG-BI) 2020 ,		4
35	Switched-capacitor-based boost multilevel inverter topology with higher voltage gain. <i>IET Power Electronics</i> , 2020 , 13, 3209-3212	2.2	9
34	A Reduced Switch Count Boost Inverter (RSC- BI) Topology with Triple Voltage Gain 2020 ,		2
33	Seven-Level Switched-Capacitor Based Multilevel Inverter With Lesser Number of Power Electronic Components and Reduced Voltage Stress 2020 ,		1
32	Single-Phase 9L Switched-Capacitor Boost Multilevel Inverter (9L-SC-BMLI) Topology 2020 ,		2
31	New switched-capacitor-based boost inverter topology with reduced switch count. <i>Journal of Power Electronics</i> , 2020 , 20, 926-937	0.9	7
30	7L-SCBI topology with minimal semiconductor device count. <i>IET Power Electronics</i> , 2020 , 13, 3199-3203	2.2	10
29	Reduced switch count-based N -level boost inverter topology for higher voltage gain. <i>IET Power Electronics</i> , 2020 , 13, 3505-3509	2.2	13
28	Design and implementation of a new unity gain nine-level active neutral point clamped multilevel inverter topology. <i>IET Power Electronics</i> , 2020 , 13, 3204-3208	2.2	10
27	Single-phase hybrid multilevel inverter topology with low switching frequency modulation techniques for lower order harmonic elimination. <i>IET Power Electronics</i> , 2020 , 13, 4117-4127	2.2	7

26	A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology With Reduced Switch Count. <i>IEEE Access</i> , 2020 , 8, 5840-5851	3.5	36
25	. <i>IEEE Access</i> , 2020 , 8, 201835-201846	3.5	14
24	A Novel Switched-Capacitor Multilevel Inverter Topology for Energy Storage and Smart Grid Applications. <i>Electronics (Switzerland)</i> , 2020 , 9, 1703	2.6	13
23	. <i>IEEE Access</i> , 2020 , 8, 188726-188741	3.5	20
22	An improved asymmetrical multilevel inverter topology with reduced semiconductor device count. <i>International Transactions on Electrical Energy Systems</i> , 2020 , 30, e12587	2.2	12
21	A New Eight Switch Seven Level Boost Active Neutral Point Clamped (8S-7L-BANPC) Inverter. <i>IEEE Access</i> , 2020 , 8, 203972-203981	3.5	8
20	A New Seven-Level Inverter Topology with Reduced Switch Number 2020 ,		1
19	A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress. <i>International Transactions on Electrical Energy Systems</i> , 2020 , 30, e12191	2.2	21
18	A New Switched Capacitor 7L Inverter With Triple Voltage Gain and Low Voltage Stress. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020 , 67, 1294-1298	3.5	56
17	Reduced Switch Count Based Single Source 7L Boost Inverter Topology. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020 , 67, 3252-3256	3.5	27
16	Design and Implementation of a Hybrid Single T-Type Double H-Bridge Multilevel Inverter (STDH-MLI) Topology. <i>Energies</i> , 2019 , 12, 1810	3.1	14
15	A New Multilevel Inverter Topology With Reduce Switch Count. <i>IEEE Access</i> , 2019 , 7, 58584-58594	3.5	82
14	Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count. <i>IEEE Access</i> , 2019 , 7, 24498-24510	3.5	117
13	Low Switching Frequency Based Asymmetrical Multilevel Inverter Topology With Reduced Switch Count. <i>IEEE Access</i> , 2019 , 7, 86374-86383	3.5	72
12	A Quasi Impedance Source Inverter based Wireless Power Transfer System for Battery Charging Applications for Electric Vehicle 2019 ,		3
11	Comparative Analysis of Optimal and Fixed Input DC Sources with Selective Harmonic Elimination Pulse Width Modulation 2019 ,		6
10	SHEPWM Based New Hybrid Multilevel Inverter Topology with Reduced Switch Count 2019 ,		1
9	A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress. <i>IEEE Access</i> , 2019 , 7, 174178-174188	3.5	46

8	A New Single-Phase Single Source Nine Level Boost Inverter Topology 2019 ,		2
7	Single phase symmetrical and asymmetrical design of multilevel inverter topology with reduced number of switches 2018 ,		7
6	Asymmetrical Multilevel Inverter Topology with Reduced Number of Components 2018 ,		6
5	Performance analysis of carrier based PWM technique for three level diode clamped multilevel inverter with different reference signals 2016 ,		7
4	A switched-capacitor multilevel inverter topology employing a novel variable structure nearest-level modulation. <i>International Transactions on Electrical Energy Systems</i> ,e13151	2.2	2
3	A non-isolated quasi-Z-source-based high-gain DCDC converter. <i>International Journal of Circuit Theory and Applications</i> ,	2	1
2	Analysis and implementation of a new asymmetric double H-bridge multilevel inverter. <i>International Journal of Circuit Theory and Applications</i> ,	2	2
1	A high gain noninverting DCDC converter with low voltage stress for industrial applications. <i>International Journal of Circuit Theory and Applications</i> ,	2	2