Marif Daula Siddique

List of Publications by Citations

61 papers	889 citations	14 h-index	27 g-index
68 ext. papers	1,482 ext. citations	2.8 avg, IF	5.35 L-index

#	Paper	IF	Citations
61	Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count. *IEEE Access*, **2019**, 7, 24498-24510	3.5	117
60	A New Multilevel Inverter Topology With Reduce Switch Count. *IEEE Access*, **2019**, 7, 58584-58594	3.5	82
59	Low Switching Frequency Based Asymmetrical Multilevel Inverter Topology With Reduced Switch Count. *IEEE Access*, **2019**, 7, 86374-86383	3.5	72
58	A New Switched Capacitor 7L Inverter With Triple Voltage Gain and Low Voltage Stress. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1294-1298	3.5	56
57	A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress. *IEEE Access*, **2019**, 7, 174178-174188	3.5	46
56	Single-Phase Step-Up Switched-Capacitor-Based Multilevel Inverter Topology With SHEPWM. *IEEE Transactions on Industry Applications*, **2021**, 57, 3107-3119	4.3	42
55	A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology With Reduced Switch Count. *IEEE Access*, **2020**, 8, 5840-5851	3.5	36
54	Dual input switched-capacitor-based single-phase hybrid boost multilevel inverter topology with reduced number of components. *IET Power Electronics*, **2020**, 13, 881-891	2.2	31
53	Asynchronous Particle Swarm Optimization-Genetic Algorithm (APSO-GA) based Selective Harmonic Elimination in a Cascaded H-Bridge Multilevel Inverter. *IEEE Transactions on Industrial Electronics*, **2021**, 1-1	8.9	30
52	Reduced Switch Count Based Single Source 7L Boost Inverter Topology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3252-3256	3.5	27
51	Dual asymmetrical dc voltage source based switched capacitor boost multilevel inverter topology. *IET Power Electronics*, **2020**, 13, 1481-1486	2.2	23
50	A new single-phase cascaded multilevel inverter topology with reduced number of switches and voltage stress. *International Transactions on Electrical Energy Systems*, **2020**, 30, e12191	2.2	21
49	. *IEEE Access*, **2020**, 8, 188726-188741	3.5	20
48	Quadruple Boost Multilevel Inverter (QB-MLI) Topology With Reduced Switch Count. *IEEE Transactions on Power Electronics*, **2021**, 36, 7372-7377	7.2	15
47	Design and Implementation of a Hybrid Single T-Type Double H-Bridge Multilevel Inverter (STDH-MLI) Topology. *Energies*, **2019**, 12, 1810	3.1	14
46	. *IEEE Access*, **2020**, 8, 201835-201846	3.5	14
45	Reduced switch count-based N -level boost inverter topology for higher voltage gain. *IET Power Electronics*, **2020**, 13, 3505-3509	2.2	13

44	A Novel Switched-Capacitor Multilevel Inverter Topology for Energy Storage and Smart Grid Applications. *Electronics (Switzerland)*, **2020**, 9, 1703	2.6	13
43	A New Family of Step-Up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies With Dual Input Voltage Sources. *IEEE Access*, **2021**, 9, 4398-4410	3.5	13
42	An improved asymmetrical multilevel inverter topology with reduced semiconductor device count. *International Transactions on Electrical Energy Systems*, **2020**, 30, e12587	2.2	12
41	Recent trends and review on switched-capacitor-based single-stage boost multilevel inverter. *International Transactions on Electrical Energy Systems*, **2021**, 31, e12730	2.2	12
40	Compact Seven-Level Boost Type Inverter Topology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1358-1362	3.5	11
39	7L-SCBI topology with minimal semiconductor device count. *IET Power Electronics*, **2020**, 13, 3199-3203	2.2	10
38	Design and implementation of a new unity gain nine-level active neutral point clamped multilevel inverter topology. *IET Power Electronics*, **2020**, 13, 3204-3208	2.2	10
37	A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources. *International Journal of Electrical Power and Energy Systems*, **2021**, 128, 106730	5.1	10
36	Switched-capacitor-based boost multilevel inverter topology with higher voltage gain. *IET Power Electronics*, **2020**, 13, 3209-3212	2.2	9
35	A transformerless high gain dc□dc boost converter with reduced voltage stress. *International Transactions on Electrical Energy Systems*, **2021**, 31, e12877	2.2	9
34	A New Eight Switch Seven Level Boost Active Neutral Point Clamped (8S-7L-BANPC) Inverter. *IEEE Access*, **2020**, 8, 203972-203981	3.5	8
33	Performance analysis of carrier based PWM technique for three level diode clamped multilevel inverter with different reference signals **2016**,		7
32	Single phase symmetrical and asymmetrical design of multilevel inverter topology with reduced number of switches **2018**,		7
31	New switched-capacitor-based boost inverter topology with reduced switch count. *Journal of Power Electronics*, **2020**, 20, 926-937	0.9	7
30	Single-phase hybrid multilevel inverter topology with low switching frequency modulation techniques for lower order harmonic elimination. *IET Power Electronics*, **2020**, 13, 4117-4127	2.2	7
29	Single-Phase Boost Switched-Capacitor Based Multilevel Inverter Topology with Reduced Switching Devices. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **2021**, 1-1	5.6	6
28	Comparative Analysis of Optimal and Fixed Input DC Sources with Selective Harmonic Elimination Pulse Width Modulation **2019**,		6
27	Implementation and Analysis of a 15-Level Inverter Topology With Reduced Switch Count. *IEEE Access*, **2021**, 9, 40623-40634	3.5	6

26	Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count. *International Journal of Circuit Theory and Applications*, **2021**, 49, 1757-1775	2	6
25	Asymmetrical Multilevel Inverter Topology with Reduced Number of Components **2018**,		6
24	Experimental validation of new self-voltage balanced 9L-ANPC inverter for photovoltaic applications. *Scientific Reports*, **2021**, 11, 5067	4.9	5
23	A Cross Connected Asymmetrical Switched-Capacitor Multilevel Inverter. *IEEE Access*, **2021**, 9, 96416-96429	3.9	5
22	A New Multilevel Inverter Topology with Reduced DC Sources. *Energies*, **2021**, 14, 4709	3.1	5
21	Switched-Capacitor Based Seven-Level Triple Voltage Gain Boost Inverter (7L-TVG-BI) **2020**,		4
20	An improved asymmetrical multi-level inverter topology with boosted output voltage and reduced components count. *IET Power Electronics*, **2021**, 14, 2052-2066	2.2	4
19	Experimental validation of nine-level switched-capacitor inverter topology with high voltage gain. *International Journal of Circuit Theory and Applications*, **2021**, 49, 2479	2	3
18	A twice boost nine-level switched-capacitor multilevel (2B-9L-SCMLI) inverter with self-voltage balancing capability. *International Journal of Circuit Theory and Applications*, **2021**, 49, 2578	2	3
17	A Quasi Impedance Source Inverter based Wireless Power Transfer System for Battery Charging Applications for Electric Vehicle **2019**,		3
16	A 9 and 13-Level Switched-Capacitor-Based Multilevel Inverter with enhanced Self-Balanced Capacitor Voltage Capability. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, **2022**, 1-1	5.6	3
15	New Switched-Capacitor based Boost Seven-Level ANPC (7L-ANPC) Boost Inverter Topology **2020**,		2
14	A switched-capacitor multilevel inverter topology employing a novel variable structure nearest-level modulation. *International Transactions on Electrical Energy Systems*,e13151	2.2	2
13	A Reduced Switch Count Boost Inverter (RSC- BI) Topology with Triple Voltage Gain **2020**,		2
12	Single-Phase 9L Switched-Capacitor Boost Multilevel Inverter (9L-SC-BMLI) Topology **2020**,		2
11	A new family of boost active neutral point clamped inverter topology with reduced switch count. *IET Power Electronics*, **2021**, 14, 1433-1443	2.2	2
10	Analysis and implementation of a new asymmetric double H-bridge multilevel inverter. *International Journal of Circuit Theory and Applications*,	2	2
9	A New Single-Phase Single Source Nine Level Boost Inverter Topology **2019**,		2

List of Publications

8	A high gain noninverting DCDC converter with low voltage stress for industrial applications. *International Journal of Circuit Theory and Applications*,	2	2
7	A non-isolated quasi-Z-source-based high-gain DCDC converter. *International Journal of Circuit Theory and Applications*,	2	1
6	Seven-Level Switched-Capacitor Based Multilevel Inverter With Lesser Number of Power Electronic Components and Reduced Voltage Stress **2020**,		1
5	A New Seven-Level Inverter Topology with Reduced Switch Number **2020**,		1
4	SHEPWM Based New Hybrid Multilevel Inverter Topology with Reduced Switch Count **2019**,		1
3	A New Configuration of Nine-Level Boost Inverter with Reduced Component Count. *E-Prime*, **2021**, 1, 100010		0
2	An Improved 15-Level Asymmetrical Multilevel Inverter with Reduced Switch Count. *Lecture Notes in Electrical Engineering*, **2021**, 709-718	0.2	0
1	Compact Quadratic Boost Switched-Capacitor Inverter. *IEEE Transactions on Industry Applications*, **2022**, 1-1	4.3	0