Marif Daula Siddique

List of Publications by Year
in descending order

66	2,076	257101 24	264894 42
papers	citations	h-index	g-index

68	68	68	641
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count. IEEE Access, 2019, 7, 24498-24510.	2.6	207
2	A New Multilevel Inverter Topology With Reduce Switch Count. IEEE Access, 2019, 7, 58584-58594.	2.6	155
3	Low Switching Frequency Based Asymmetrical Multilevel Inverter Topology With Reduced Switch Count. IEEE Access, 2019, 7, 86374-86383.	2.6	117
4	A New Switched Capacitor 7L Inverter With Triple Voltage Gain and Low Voltage Stress. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1294-1298.	2.2	106
5	Asynchronous Particle Swarm Optimization-Genetic Algorithm (APSO-GA) Based Selective Harmonic Elimination in a Cascaded H-Bridge Multilevel Inverter. IEEE Transactions on Industrial Electronics, 2022, 69, 1477-1487.	5.2	96
6	Single-Phase Step-Up Switched-Capacitor-Based Multilevel Inverter Topology With SHEPWM. IEEE Transactions on Industry Applications, 2021, 57, 3107-3119.	3.3	95
7	A New Single Phase Single Switched-Capacitor Based Nine-Level Boost Inverter Topology With Reduced Switch Count and Voltage Stress. IEEE Access, 2019, 7, 174178-174188.	2.6	90
8	A Single DC Source Nine-Level Switched-Capacitor Boost Inverter Topology With Reduced Switch Count. IEEE Access, 2020, 8, 5840-5851.	2.6	61
9	A New Configurable Topology for Multilevel Inverter With Reduced Switching Components. IEEE Access, 2020, 8, 188726-188741.	2.6	56
10	Reduced Switch Count Based Single Source 7L Boost Inverter Topology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3252-3256.	2.2	54
11	Dual asymmetrical dc voltage source based switched capacitor boost multilevel inverter topology. IET Power Electronics, 2020, 13, 1481-1486.	1.5	48
12	Dual input switchedâ€capacitorâ€based singleâ€phase hybrid boost multilevel inverter topology with reduced number of components. IET Power Electronics, 2020, 13, 881-891.	1.5	48
13	A new singleâ€phase cascaded multilevel inverter topology with reduced number of switches and voltage stress. International Transactions on Electrical Energy Systems, 2020, 30, e12191.	1.2	44
14	Quadruple Boost Multilevel Inverter (QB-MLI) Topology With Reduced Switch Count. IEEE Transactions on Power Electronics, 2021, 36, 7372-7377.	5.4	42
15	Extended Multilevel Inverter Topology With Reduced Switch Count and Voltage Stress. IEEE Access, 2020, 8, 201835-201846.	2.6	40
16	A New Family of Step-Up Hybrid Switched-Capacitor Integrated Multilevel Inverter Topologies With Dual Input Voltage Sources. IEEE Access, 2021, 9, 4398-4410.	2.6	39
17	A transformerless high gain <scp>dcâ€“dc</scp> boost converter with reduced voltage stress. International Transactions on Electrical Energy Systems, 2021, 31, e12877.	1.2	35
18	A high gain noninverting DCâ€“DC converter with low voltage stress for industrial applications. International Journal of Circuit Theory and Applications, 2021, 49, 4212-4230.	1.3	35

#	Article	IF	Citations
19	Recent trends and review on<scp>switchedâ€capacitor</scp>â€based<scp>singleâ€stage</scp>boost multilevel inverter. International Transactions on Electrical Energy Systems, 2021, 31, e12730.	1.2	33
20	An improved asymmetrical multilevel inverter topology with reduced semiconductor device count. International Transactions on Electrical Energy Systems, 2020, 30, e12587.	1.2	32
21	A New Eight Switch Seven Level Boost Active Neutral Point Clamped (8S-7L-BANPC) Inverter. IEEE Access, 2020, 8, 203972-203981.	2.6	30
22	A new cascaded asymmetrical multilevel inverter based on switched dc voltage sources. International Journal of Electrical Power and Energy Systems, 2021, 128, 106730.	3.3	30
23	A Novel Switched-Capacitor Multilevel Inverter Topology for Energy Storage and Smart Grid Applications. Electronics (Switzerland), 2020, 9, 1703.	1.8	28
24	Single-Phase Boost Switched-Capacitor-Based Multilevel Inverter Topology With Reduced Switching Devices. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022, 10, 4336-4346.	3.7	28
25	Implementation and Analysis of a 15-Level Inverter Topology With Reduced Switch Count. IEEE Access, 2021, 9, 40623-40634.	2.6	25
26	A nonâ€isolated quasiâ€Zâ€sourceâ€based highâ€gain DCâ€“DC converter. International Journal of Circuit Theory and Applications, 2022, 50, 653-682.	1.3	25
27	Compact Seven-Level Boost Type Inverter Topology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1358-1362.	2.2	24
28	Experimental validation of new self-voltage balanced 9L-ANPC inverter for photovoltaic applications. Scientific Reports, 2021, 11, 5067.	1.6	24
29	Design and implementation of a new unity gain nineâ€level active neutral point clamped multilevel inverter topology. IET Power Electronics, 2020, 13, 3204-3208.	1.5	24
30	A twice boost nineâ€level switchedâ€capacitor multilevel (2Bâ€9Lâ€SCMLI) inverter with selfâ€voltage balancing capability. International Journal of Circuit Theory and Applications, 2021, 49, 2578-2592.	1.3	23
31	Reduced switch countâ€based N â€level boost inverter topology for higher voltage gain. IET Power Electronics, 2020, 13, 3505-3509.	1.5	23
32	Design and Implementation of a Hybrid Single T-Type Double H-Bridge Multilevel Inverter (STDH-MLI) Topology. Energies, 2019, 12, 1810.	1.6	21
33	Asymmetrical multilevel inverter topology with low total standing voltage and reduced switches count. International Journal of Circuit Theory and Applications, 2021, 49, 1757-1775.	1.3	21
34	An improved asymmetrical multiâ€level inverter topology with boosted output voltage and reduced components count. IET Power Electronics, 2021, 14, 2052-2066.	1.5	21
35	New switched-capacitor-based boost inverter topology with reduced switch count. Journal of Power Electronics, 2020, 20, 926-937.	0.9	20
36	A Cross Connected Asymmetrical Switched-Capacitor Multilevel Inverter. IEEE Access, 2021, 9, 96416-96429.	2.6	19

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37	Switchedâ€capacitorâ€based boost multilevel inverter topology with higher voltage gain. IET Power Electronics, 2020, 13, 3209-3212.	1.5	19
38	A 9- and 13-Level Switched-Capacitor-Based Multilevel Inverter With Enhanced Self-Balanced Capacitor Voltage Capability. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2022, 10, 7225-7237.	3.7	19
39	7Lâ€SCBI topology with minimal semiconductor device count. IET Power Electronics, 2020, 13, 3199-3203.	1.5	15
40	Ultra high gain step up DC/DC converter based on switched inductor and improved voltage lift technique for highâ€voltage applications. IET Power Electronics, 2022, 15, 932-952.	1.5	14
41	Single phase symmetrical and asymmetrical design of multilevel inverter topology with reduced number of switches. , 2018, , .		13
42	Experimental validation of nineâ€level switchedâ€capacitor inverter topology with high voltage gain. International Journal of Circuit Theory and Applications, 2021, 49, 2479-2493.	1.3	13
43	A New Multilevel Inverter Topology with Reduced DC Sources. Energies, 2021, 14, 4709.	1.6	13
44	Compact Quadratic Boost Switched-Capacitor Inverter. IEEE Transactions on Industry Applications, 2022, 58, 4923-4931.	3.3	13
45	Singleâ€phase hybrid multilevel inverter topology with low switching frequency modulation techniques for lower order harmonic elimination. IET Power Electronics, 2020, 13, 4117-4127.	1.5	12
46	Performance analysis of carrier based PWM technique for three level diode clamped multilevel inverter with different reference signals. , 2016, , .		11
47	Analysis and implementation of a new asymmetric double Hâ€bridge multilevel inverter. International Journal of Circuit Theory and Applications, 2021, 49, 4012-4026.	1.3	11
48	A <scp>switchedâ€capacitor</scp> multilevel inverter topology employing a novel variable structure nearestâ€level modulation. International Transactions on Electrical Energy Systems, 2021, 31, e13151.	1.2	11
49	Asymmetrical Multilevel Inverter Topology with Reduced Number of Components. , 2018, , .		10
50	Comparative Analysis of Optimal and Fixed Input DC Sources with Selective Harmonic Elimination Pulse Width Modulation. , 2019, , .		9
51	A new family of boost active neutral point clamped inverter topology with reduced switch count. IET Power Electronics, 2021, 14, 1433-1443.	1.5	8
52	A new highâ€level boost inverter topology with reduced device count. International Journal of Circuit Theory and Applications, 2022, 50, 2777-2792.	1.3	8
53	A new sevenâ€level ANPC inverter structure with semiconductor device reduction. International Journal of Circuit Theory and Applications, 2022, 50, 2660-2670.	1.3	8
54	Switched-Capacitor Based Seven-Level Triple Voltage Gain Boost Inverter (7L-TVG-BI). , 2020, , .		7

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55	Single-Phase 9L Switched-Capacitor Boost Multilevel Inverter (9L-SC-BMLI) Topology. , 2020, , .		7
56	New Switched-Capacitor based Boost Seven-Level ANPC (7L-ANPC) Boost Inverter Topology. , 2020, , .		6
57	A Quasi Impedance Source Inverter based Wireless Power Transfer System for Battery Charging Applications for Electric Vehicle. , 2019, , .		5
58	A New Single-Phase Single Source Nine Level Boost Inverter Topology. , 2019, , .		5
59	Seven-Level Switched-Capacitor Based Multilevel Inverter With Lesser Number of Power Electronic Components and Reduced Voltage Stress. , 2020, , .		4
60	A High Gain 9L Switched-Capacitor Boost Inverter (9L-SCMI) With Reduced Component Count. , 2021, , .		3
61	A Reduced Switch Count Boost Inverter (RSC- BI) Topology with Triple Voltage Gain. , 2020, , .		3
62	11 Level boost inverter topology with dualâ€source configuration. IET Power Electronics, 2023, 16, 1696-1702.	1.5	3
63	SHEPWM Based New Hybrid Multilevel Inverter Topology with Reduced Switch Count. , 2019, , .		2
64	An Improved 15-Level Asymmetrical Multilevel Inverter with Reduced Switch Count. Lecture Notes in Electrical Engineering, 2021, , 709-718.	0.3	2
65	A New Configuration of Nine-Level Boost Inverter with Reduced Component Count. E-Prime, 2021, 1, 100010.	2.1	2
66	A New Seven-Level Inverter Topology with Reduced Switch Number. , 2020, , .		1