Taizhi Liu

List of Publications by Year
in descending order

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26 papers	210 citations	1307594 7 h-index	1199594 12 g-index
26 all docs	26 docs citations	26 times ranked	115 citing authors

#	Article	IF	Citations
1	System-level variation-aware aging simulator using a unified novel gate-delay model for bias temperature instability, hot carrier injection, and gate oxide breakdown. Microelectronics Reliability, 2015, 55, 1334-1340.	1.7	25
2	System-level modeling of microprocessor reliability degradation due to BTI and HCI. , 2014, , .		21
3	SRAM stability analysis for different cache configurations due to Bias Temperature Instability and Hot Carrier Injection. , 2016, , .		18
4	System-Level Modeling of Microprocessor Reliability Degradation Due to Bias Temperature Instability and Hot Carrier Injection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2712-2725.	3.1	17
5	Comprehensive reliability and aging analysis on SRAMs within microprocessor systems. Microelectronics Reliability, 2015, 55, 1290-1296.	1.7	15
6	Comprehensive Reliability-Aware Statistical Timing Analysis Using a Unified Gate-Delay Model for Microprocessors. IEEE Transactions on Emerging Topics in Computing, 2018, 6, 219-232.	4.6	15
7	A Comprehensive Time-Dependent Dielectric Breakdown Lifetime Simulator for Both Traditional CMOS and FinFET Technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2470-2482.	3.1	14
8	Accurate standard cell characterization and statistical timing analysis using multivariate adaptive regression splines. , 2015, , .		10
9	Front-end of line and middle-of-line time-dependent dielectric breakdown reliability simulator for logic circuits. Microelectronics Reliability, 2017, 76-77, 81-86.	1.7	9
10	Extraction of threshold voltage degradation modeling due to Negative Bias Temperature Instability in circuits with I/O measurements. , 2014, , .		7
11	Analysis of time-dependent dielectric breakdown induced aging of SRAM cache with different configurations. Microelectronics Reliability, 2017, 76-77, 87-91.	1.7	7
12	SRAM Stability Analysis and Performanceâ€"Reliability Tradeoff for Different Cache Configurations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 620-633.	3.1	7
13	Negative Bias Temperature Instability and Gate Oxide Breakdown Modeling in Circuits With Die-to-Die Calibration Through Power Supply and Ground Signal Measurements. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2271-2284.	3.1	6
14	Circuit-level reliability simulator for front-end-of-line and middle-of-line time-dependent dielectric breakdown in FinFET technology. , 2018, , .		6
15	Modeling for SRAM reliability degradation due to gate oxide breakdown with a compact current model. , 2017, , .		5
16	Modeling of the reliability degradation of a FinFET-based SRAM due to bias temperature instability, hot carrier injection, and gate oxide breakdown. , 2017, , .		5
17	Impact of front-end wearout mechanisms on FinFET SRAM soft error rate. Microelectronics Reliability, 2019, 100-101, 113487.	1.7	5
18	A lifetime and power sensitive design optimization framework for a radio frequency circuit. , 2017, , .		3

#	Article	IF	Citations
19	Estimation of the Optimal Accelerated Test Region for FinFET SRAMs Degraded by Front-End and Back-End Wearout Mechanisms. , 2018, , .		3
20	Impact of Front-End Wearout Mechanisms on the Performance of a Ring Oscillator-Based Thermal Sensor. , 2019, , .		3
21	A Comprehensive Framework for Analysis of Time-Dependent Performance-Reliability Degradation of SRAM Cache Memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 857-870.	3.1	3
22	Optimal Accelerated Test Regions for Time- Dependent Dielectric Breakdown Lifetime Parameters Estimation in FinFET Technology. , 2018, , .		2
23	A library based on deep neural networks for modeling the degradation of FinFET SRAM performance metrics due to aging. Microelectronics Reliability, 2019, 100-101, 113486.	1.7	2
24	Design for reliability: A duty-cycle management system for timing violations. , 2016, , .		1
25	Inverse Design of FinFET SRAM Cells. , 2020, , .		1
26	New Electromigration Model and Its Potential Application on Degradation Simulation for FinFET SRAM. , 2018, , .		0