Kaushik

List of Publications by Citations

368 papers	9,423 citations	50 h-index	82 g-index
407 ext. papers	12,048 ext. citations	3.5 avg, IF	6.93 L-index

#	Paper	IF	Citations
368	Low-Power Digital Signal Processing Using Approximate Adders. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2013**, 32, 124-137	2.5	401
367	Analysis and characterization of inherent application resilience for approximate computing **2013**,		284
366	A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM. *IEEE Journal of Solid-State Circuits*, **2007**, 42, 2303-2313	5.5	283
365	A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS. *IEEE Journal of Solid-State Circuits*, **2009**, 44, 650-658	5.5	275
364	Going Deeper in Spiking Neural Networks: VGG and Residual Architectures. *Frontiers in Neuroscience*, **2019**, 13, 95	5.1	207
363	IMPACT: IMPrecise adders for low-power approximate computing **2011**,		204
362	SALSA **2012**,		201
361	Quality programmable vector processors for approximate computing **2013**,		162
360	Hardware Trojan Detection by Multiple-Parameter Side-Channel Analysis. *IEEE Transactions on Computers*, **2013**, 62, 2183-2195	2.5	144
359	AxNN **2014**,		134
358	MACACO: Modeling and analysis of circuits for approximate computing **2011**,		128
357	Computing in Memory With Spin-Transfer Torque Magnetic RAM. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 470-483	2.6	123
356	Spin-Based Neuron Model With Domain-Wall Magnets as Synapse. *IEEE Nanotechnology Magazine*, **2012**, 11, 843-853	2.6	120
355	Magnetic Tunnel Junction Based Long-Term Short-Term Stochastic Synapse for a Spiking Neural Network with On-Chip STDP Learning. *Scientific Reports*, **2016**, 6, 29545	4.9	119
354	Design of voltage-scalable meta-functions for approximate computing **2011**,		118
353	Spin-Transfer Torque Devices for Logic and Memory: Prospects and Perspectives. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1-22	2.5	114
352	Scalable effort hardware design **2010**,		114

351	Proposal for an All-Spin Artificial Neural Network: Emulating Neural and Synaptic Functionalities Through Domain Wall Motion in Ferromagnets. *IEEE Transactions on Biomedical Circuits and Systems* , **2016**, 10, 1152-1160	5.1	109
350	PUMA **2019**,		107
349	Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 319-332	2.6	107
348	KNACK: A hybrid spin-charge mixed-mode simulator for evaluating different genres of spin-transfer torque MRAM bit-cells **2011**,		104
347	Magnetic Tunnel Junction Mimics Stochastic Cortical Spiking Neurons. *Scientific Reports*, **2016**, 6, 30039	4.9	93
346	Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) From Circuit/Architecture Perspective. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 1710-1723	2.6	89
345	Substitute-and-simplify: A unified design paradigm for approximate and quality configurable circuits **2013**,		83
344	X-SRAM: Enabling In-Memory Boolean Computations in CMOS Static Random Access Memories. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 4219-4232	3.9	82
343	Efficient Design of Micro-Scale Energy Harvesting Systems. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2011**, 1, 254-266	5.2	77
342	Asymmetric Drain Spacer Extension (ADSE) FinFETs for Low-Power and Robust SRAMs. *IEEE Transactions on Electron Devices*, **2011**, 58, 296-308	2.9	75
341	Probabilistic Deep Spiking Neural Systems Enabled by Magnetic Tunnel Junction. *IEEE Transactions on Electron Devices*, **2016**, 63, 2963-2970	2.9	73
340	Bit-Cell Level Optimization for Non-volatile Memories Using Magnetic Tunnel Junctions and Spin-Transfer Torque Switching. *IEEE Nanotechnology Magazine*, **2012**, 11, 172-181	2.6	72
339	Enabling Spike-Based Backpropagation for Training Deep Neural Network Architectures. *Frontiers in Neuroscience*, **2020**, 14, 119	5.1	71
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332	Dynamic Bit-Width Adaptation in DCT: An Approach to Trade Off Image Quality and Computation Energy. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2010**, 18, 787-793	2.6	63
331	Tree-CNN: A hierarchical Deep Convolutional Neural Network for incremental learning. *Neural Networks*, **2020**, 121, 148-160	9.1	63
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329	Multilevel Spin-Orbit Torque MRAMs. *IEEE Transactions on Electron Devices*, **2015**, 62, 561-568	2.9	62
328	Significance driven computation **2009**,		62
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324	Exploring Asynchronous Design Techniques for Process-Tolerant and Energy-Efficient Subthreshold Operation. *IEEE Journal of Solid-State Circuits*, **2010**, 45, 401-410	5.5	53
323	Analytical Subthreshold Potential Distribution Model for Gate Underlap Double-Gate MOS Transistors. *IEEE Transactions on Electron Devices*, **2007**, 54, 1793-1798	2.9	53
322	An All-Memristor Deep Spiking Neural Computing System: A Step Toward Realizing the Low-Power Stochastic Brain. *IEEE Transactions on Emerging Topics in Computational Intelligence*, **2018**, 2, 345-358	4.1	53
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319	Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 1957-1966	2.5	50
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317	Negative Bias Temperature Instability: Estimation and Design for Improved Reliability of Nanoscale Circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 743-751	2.5	48
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315	Layout-aware optimization of stt mrams **2012**,		45
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312	Unsupervised regenerative learning of hierarchical features in Spiking Deep Networks for object recognition **2016**,		43
311	Scalable Effort Hardware Design. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2004-2016	2.6	43
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