Kaushik

List of Publications by Year
in descending order

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406	14,599	30047	43868
papers	citations	54	91
		h-index	g-index

407	407	407	7191
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Low-Power Digital Signal Processing Using Approximate Adders. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 124-137.	1.9	606
2	Going Deeper in Spiking Neural Networks: VGG and Residual Architectures. Frontiers in Neuroscience, 2019, 13, 95.	1.4	573
3	Analysis and characterization of inherent application resilience for approximate computing. , 2013, , .		393
4	A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM. IEEE Journal of Solid-State Circuits, 2007, 42, 2303-2313.	3.5	380
5	A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2009, 44, 650-658.	3.5	366
6	IMPACT: IMPrecise adders for low-power approximate computing. , 2011, , .		291
7	SALSA. , 2012, , .		274
8	PUMA. , 2019, , .		242
9	Computing in Memory With Spin-Transfer Torque Magnetic RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 470-483.	2.1	235
10	Roadmap of Spinâ€“Orbit Torques. IEEE Transactions on Magnetics, 2021, 57, 1-39.	1.2	225
11	AxNN. , 2014, , .		203
12	Quality programmable vector processors for approximate computing. , 2013, , .		200
13	Enabling Spike-Based Backpropagation for Training Deep Neural Network Architectures. Frontiers in Neuroscience, 2020, 14, 119.	1.4	196
14	Hardware Trojan Detection by Multiple-Parameter Side-Channel Analysis. IEEE Transactions on Computers, 2013, 62, 2183-2195.	2.4	193
15	X-SRAM: Enabling In-Memory Boolean Computations in CMOS Static Random Access Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 4219-4232.	3.5	182
16	MACACO: Modeling and analysis of circuits for approximate computing. , 2011, , .		175
17	Ultralow-Voltage Process-Variation-Tolerant Schmitt-Trigger-Based SRAM Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 319-332.	2.1	162
18	Magnetic Tunnel Junction Based Long-Term Short-Term Stochastic Synapse for a Spiking Neural Network with On-Chip STDP Learning. Scientific Reports, 2016, 6, 29545.	1.6	162

#	Article	IF	Citations
19	Design of voltage-scalable meta-functions for approximate computing. , 2011, , .		159
20	Spin-Based Neuron Model With Domain-Wall Magnets as Synapse. IEEE Nanotechnology Magazine, 2012, 11, 843-853.	1.1	154
21	Spin-Transfer Torque Devices for Logic and Memory: Prospects and Perspectives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1-22.	1.9	153
22	Scalable effort hardware design. , 2010, , .		143
23	Proposal for an All-Spin Artificial Neural Network: Emulating Neural and Synaptic Functionalities Through Domain Wall Motion in Ferromagnets. IEEE Transactions on Biomedical Circuits and Systems, 2016, 10, 1152-1160.	2.7	141
24	Tree-CNN: A hierarchical Deep Convolutional Neural Network for incremental learning. Neural Networks, 2020, 121, 148-160.	3.3	138
25	Toward Fast Neural Computing using All-Photonic Phase Change Spiking Neurons. Scientific Reports, 2018, 8, 12980.	1.6	132
26	Magnetic Tunnel Junction Mimics Stochastic Cortical Spiking Neurons. Scientific Reports, 2016, 6, 30039.	1.6	125
27	Training Deep Spiking Convolutional Neural Networks With STDP-Based Unsupervised Pre-training Followed by Supervised Fine-Tuning. Frontiers in Neuroscience, 2018, 12, 435.	1.4	121
28	RMP-SNN: Residual Membrane Potential Neuron for Enabling Deeper High-Accuracy and Low-Latency Spiking Neural Network. , 2020, , .		120
29	Ultra Low-Power Clocking Scheme Using Energy Recovery and Clock Gating. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 33-44.	2.1	118
30	KNACK: A hybrid spin-charge mixed-mode simulator for evaluating different genres of spin-transfer torque MRAM bit-cells. , 2011, , .		118
31	Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) From Circuit/Architecture Perspective. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1710-1723.	2.1	114
32	Substitute-and-Simplify: A Unified Design Paradigm for Approximate and Quality Configurable Circuits. , 2013, , .		110
33	Roadmap on emerging hardware and technology for machine learning. Nanotechnology, 2021, 32, 012002.	1.3	104
34	Encoding neural and synaptic functionalities in electron spin: A pathway to efficient neuromorphic computing. Applied Physics Reviews, 2017, 4, 041105.	5.5	101
35	Efficient Design of Micro-Scale Energy Harvesting Systems. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 254-266.	2.7	99
36	Asymmetric Drain Spacer Extension (ADSE) FinFETs for Low-Power and Robust SRAMs. IEEE Transactions on Electron Devices, 2011, 58, 296-308.	1.6	93

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37	8T SRAM Cell as a Multibit Dot-Product Engine for Beyond Von Neumann Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2556-2567.	2.1	93
38	Multilevel Spin-Orbit Torque MRAMs. IEEE Transactions on Electron Devices, 2015, 62, 561-568.	1.6	91
39	Probabilistic Deep Spiking Neural Systems Enabled by Magnetic Tunnel Junction. IEEE Transactions on Electron Devices, 2016, 63, 2963-2970.	1.6	88
40	Failure Mitigation Techniques for 1T-1MTJ Spin-Transfer Torque MRAM Bit-cells. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 384-395.	2.1	84
41	Habituation based synaptic plasticity and organismic learning in a quantum perovskite. Nature Communications, 2017, 8, 240.	5.8	84
42	An All-Memristor Deep Spiking Neural Computing System: A Step Toward Realizing the Low-Power Stochastic Brain. IEEE Transactions on Emerging Topics in Computational Intelligence, 2018, 2, 345-358.	3.4	81
43	Bit-Cell Level Optimization for Non-volatile Memories Using Magnetic Tunnel Junctions and Spin-Transfer Torque Switching. IEEE Nanotechnology Magazine, 2012, 11, 172-181.	1.1	80
44	Dynamic Bit-Width Adaptation in DCT: An Approach to Trade Off Image Quality and Computation Energy. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 787-793.	2.1	78
45	Significance driven computation. , 2009, , .		76
46	Hybrid Spintronic-CMOS Spiking Neural Network with On-Chip Learning: Devices, Circuits, and Systems. Physical Review Applied, 2016, 6, .	1.5	76
47	Scalable Effort Hardware Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2004-2016.	2.1	74
48	Spin-orbit torque induced spike-timing dependent plasticity. Applied Physics Letters, 2015, 106, .	1.5	74
49	Spin orbit torque based electronic neuron. Applied Physics Letters, 2015, 106, .	1.5	71
50	Exploring Asynchronous Design Techniques for Process-Tolerant and Energy-Efficient Subthreshold Operation. IEEE Journal of Solid-State Circuits, 2010, 45, 401-410.	3.5	69
51	Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1957-1966.	1.9	68
52	IMAC: In-Memory Multi-Bit Multiplication and ACcumulation in 6T SRAM Array. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2521-2531.	3.5	67
53	SPINDLE. , 2014, , .		65
54	Xcel-RAM: Accelerating Binary Neural Networks in High-Throughput SRAM Compute Arrays. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3064-3076.	3.5	65

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55	Deep Spiking Convolutional Neural Network Trained With Unsupervised Spike-Timing-Dependent Plasticity. IEEE Transactions on Cognitive and Developmental Systems, 2019, 11, 384-394.	2.6	65
56	Negative Bias Temperature Instability: Estimation and Design for Improved Reliability of Nanoscale Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 743-751.	1.9	63
57	Analytical Subthreshold Potential Distribution Model for Gate Underlap Double-Gate MOS Transistors. IEEE Transactions on Electron Devices, 2007, 54, 1793-1798.	1.6	63
58	DWM-TAPESTRI - An Energy Efficient All-Spin Cache Using Domain Wall Shift Based Writes. , 2013, , .		63
59	Unsupervised regenerative learning of hierarchical features in Spiking Deep Networks for object recognition. , 2016, , .		63
60	Proposal for a Leaky-Integrate-Fire Spiking Neuron Based on Magnetoelectric Switching of Ferromagnets. IEEE Transactions on Electron Devices, 2017, 64, 1818-1824.	1.6	63
61	Spike-FlowNet: Event-Based Optical Flow Estimation with Energy-Efficient Hybrid Neural Networks. Lecture Notes in Computer Science, 2020, , 366-382.	1.0	62
62	Layout-aware optimization of stt mrams. , 2012, , .		61
63	Spin-neurons: A possible path to energy-efficient neuromorphic computers. Journal of Applied Physics, 2013, 114, .	1.1	61
64	Incremental Learning in Deep Convolutional Neural Networks Using Partial Network Sharing. IEEE Access, 2020, 8, 4615-4628.	2.6	61
65	RESPARC. , 2017, , .		60
66	Technology Aware Training in Memristive Neuromorphic Systems for Nonideal Synaptic Crossbars. IEEE Transactions on Emerging Topics in Computational Intelligence, 2018, 2, 335-344.	3.4	60
67	Asymmetrically Doped FinFETs for Low-Power Robust SRAMs. IEEE Transactions on Electron Devices, 2011, 58, 4241-4249.	1.6	59
68	Sensitivity analysis and optimization of thin-film thermoelectric coolers. Journal of Applied Physics, 2013, 113, 214906.	1.1	59
69	A Vision for All-Spin Neural Networks: A Device to System Perspective. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 2267-2277.	3.5	58
70	Toward Scalable, Efficient, and Accurate Deep Spiking Neural Networks With Backward Residual Connections, Stochastic Softmax, and Hybridization. Frontiers in Neuroscience, 2020, 14, 653.	1.4	58
71	Low-power functionality enhanced computation architecture using spin-based devices. , 2011, , .		56
72	A Low-Power SRAM Using Bit-Line Charge-Recycling. IEEE Journal of Solid-State Circuits, 2008, 43, 446-459.	3.5	55

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73	Resistive Crossbars as Approximate Hardware Building Blocks for Machine Learning: Opportunities and Challenges. Proceedings of the IEEE, 2020, 108, 2276-2310.	16.4	55
74	Digital Computation in Subthreshold Region for Ultralow-Power Operation: A Deviceâ€“Circuitâ€“Architecture Codesign Perspective. Proceedings of the IEEE, 2010, 98, 160-190.	16.4	54
75	PANTHER: A Programmable Architecture for Neural Network Training Harnessing Energy-Efficient ReRAM. IEEE Transactions on Computers, 2020, 69, 1128-1142.	2.4	54
76	RxNN: A Framework for Evaluating Deep Neural Networks on Resistive Crossbars. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 326-338.	1.9	54
77	Design Space Exploration of Hysteresis-Free HfZrO_x-Based Negative Capacitance FETs. IEEE Electron Device Letters, 2017, 38, 1165-1167.	2.2	52
78	1T Non-Volatile Memory Design Using Sub-10nm Ferroelectric FETs. IEEE Electron Device Letters, 2018, 39, 359-362.	2.2	52
79	SHE-NVFF: Spin Hall Effect-Based Nonvolatile Flip-Flop for Power Gating Architecture. IEEE Electron Device Letters, 2014, 35, 488-490.	2.2	51
80	GENIEx: A Generalized Approach to Emulating Non-Ideality in Memristive Xbars using Neural Networks. , 2020, , .		51
81	DIET-SNN: A Low-Latency Spiking Neural Network With <u>D</u>irect <u>I</u>nput <u>E</u>ncoding and Leakage and <u>T</u>hreshold Optimization. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 3174-3182.	7.2	51
82	Design of a Process Variation Tolerant Self-Repairing SRAM for Yield Enhancement in Nanoscaled CMOS. IEEE Journal of Solid-State Circuits, 2007, 42, 1370-1382.	3.5	50
83	Dynamic effort scaling. , 2011, , .		50
84	Approximate computing: An integrated hardware approach. , 2013, , .		50
85	STT-SNN: A Spin-Transfer-Torque Based Soft-Limiting Non-Linear Neuron for Low-Power Artificial Neural Networks. IEEE Nanotechnology Magazine, 2015, 14, 1013-1023.	1.1	50
86	Coupled Spin Torque Nano Oscillators for Low Power Neural Computation. IEEE Transactions on Magnetics, 2015, 51, 1-9.	1.2	50
87	Highly reliable memory-based Physical Unclonable Function using Spin-Transfer Torque MRAM. , 2014, , .		49
88	Stochastic Spiking Neural Networks Enabled by Magnetic Tunnel Junctions: From Nontelegraphic to Telegraphic Switching Regimes. Physical Review Applied, 2017, 8, .	1.5	49
89	DSH-MRAM: Differential Spin Hall MRAM for On-Chip Memories. IEEE Electron Device Letters, 2013, 34, 1259-1261.	2.2	48
90	GaSb-InAs n-TFET With Doped Source Underlap Exhibiting Low Subthreshold Swing at Sub-10-nm Gate-Lengths. IEEE Electron Device Letters, 2014, 35, 1221-1223.	2.2	47

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91	ReStoCNet: Residual Stochastic Binary Convolutional Spiking Neural Network for Memory-Efficient Neuromorphic Computing. Frontiers in Neuroscience, 2019, 13, 189.	1.4	46
92	Voltage Scalable High-Speed Robust Hybrid Arithmetic Units Using Adaptive Clocking. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1301-1309.	2.1	44
93	Spin-Orbit-Torque-Based Spin-Dice: A True Random-Number Generator. IEEE Magnetics Letters, 2015, 6, 1-4.	0.6	43
94	Prospects of Thin-Film Thermoelectric Devices for Hot-Spot Cooling and On-Chip Energy Harvesting. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2013, 3, 2059-2067.	1.4	41
95	A Three-Terminal Dual-Pillar STT-MRAM for High-Performance Robust Memory Applications. IEEE Transactions on Electron Devices, 2011, 58, 1508-1516.	1.6	40
96	Spin-Transfer Torque MRAMs for Low Power Memories: Perspective and Prospective. IEEE Sensors Journal, 2012, 12, 756-766.	2.4	40
97	Inherent Adversarial Robustness of Deep Spiking Neural Networks: Effects of Discrete Input Encoding and Non-linear Activations. Lecture Notes in Computer Science, 2020, , 399-414.	1.0	40
98	Effect of quantum confinement on spin transport and magnetization dynamics in dual barrier spin transfer torque magnetic tunnel junctions. Journal of Applied Physics, 2010, 108, .	1.1	39
99	Energy-Efficient Non-Boolean Computing With Spin Neurons and Resistive Memory. IEEE Nanotechnology Magazine, 2014, 13, 23-34.	1.1	38
100	Magnetic Skyrmion as a Spintronic Deep Learning Spiking Neuron Processor. IEEE Transactions on Magnetics, 2018, 54, 1-7.	1.2	38
101	Perovskite neural trees. Nature Communications, 2020, 11, 2245.	5.8	38
102	Maximum power point considerations in micro-scale solar energy harvesting systems. , 2010, , .		37
103	A Read-Disturb-Free, Differential Sensing 1R/1W Port, 8T Bitcell Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1727-1730.	2.1	37
104	ASP: Learning to Forget With Adaptive Synaptic Plasticity in Spiking Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 51-64.	2.7	37
105	Process-Variation Resilient and Voltage-Scalable DCT Architecture for Robust Low-Power Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1461-1470.	2.1	36
106	Approximate Computing: An Energy-Efficient Computing Technique for Error Resilient Applications. , 2015, , .		36
107	Comprehensive Scaling Analysis of Current Induced Switching in Magnetic Memories Based on In-Plane and Perpendicular Anisotropies. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 120-133.	2.7	36
108	Area-Efficient SOT-MRAM With a Schottky Diode. IEEE Electron Device Letters, 2016, 37, 982-985.	2.2	35

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109	Ising computation based combinatorial optimization using spin-Hall effect (SHE) induced stochastic magnetization reversal. Journal of Applied Physics, 2017, 121, .	1.1	35
110	Magnetic tunnel junction enabled all-spin stochastic spiking neural network. , 2017, , .		34
111	Analysis of Liquid Ensembles for Enhancing the Performance and Accuracy of Liquid State Machines. Frontiers in Neuroscience, 2019, 13, 504.	1.4	34
112	Boolean and non-Boolean computation with spin devices. , 2012, , .		33
113	Viterbi-Based Efficient Test Data Compression. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 610-619.	1.9	33
114	Perovskite nickelates as bio-electronic interfaces. Nature Communications, 2019, 10, 1651.	5.8	33
115	AWARE (Asymmetric Write Architecture With REdundant Blocks): A High Write Speed STT-MRAM Cache Architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 712-720.	2.1	32
116	A Low Effort Approach to Structured CNN Design Using PCA. IEEE Access, 2020, 8, 1347-1360.	2.6	32
117	FinFET Based SRAM Design for Low Standby Power Applications. , 2007, , .		30
118	Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1621-1624.	2.1	30
119	Proposal for Switching Current Reduction Using Reference Layer With Tilted Magnetic Anisotropy in Magnetic Tunnel Junctions for Spin-Transfer Torque (STT) MRAM. IEEE Transactions on Electron Devices, 2012, 59, 3054-3060.	1.6	30
120	Optimizating Emerging Nonvolatile Memories for Dual-Mode Applications: Data Storage and Key Generator. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1176-1187.	1.9	30
121	Learning to Generate Sequences with Combination of Hebbian and Non-hebbian Plasticity in Recurrent Spiking Neural Networks. Frontiers in Neuroscience, 2017, 11, 693.	1.4	30
122	A Comprehensive Analysis on Adversarial Robustness of Spiking Neural Networks. , 2019, , .		30
123	Discretization Based Solutions for Secure Machine Learning Against Adversarial Attacks. IEEE Access, 2019, 7, 70157-70168.	2.6	30
124	Organismic materials for beyond von Neumann machines. Applied Physics Reviews, 2020, 7, .	5.5	30
125	Low-Overhead Maximum Power Point Tracking for Micro-Scale Solar Energy Harvesting Systems. , 2012, , .		29
126	Stochastic Spin-Orbit Torque Devices as Elements for Bayesian Inference. Scientific Reports, 2017, 7, 14101.	1.6	29

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127	Fast Tag Comparator Using Diode Partitioned Domino for 64-bit Microprocessors. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2007, 54, 322-328.	0.1	28
128	Analysis of Options in Double-Gate MOS Technology: A Circuit Perspective. IEEE Transactions on Electron Devices, 2007, 54, 3361-3368.	1.6	28
129	R-MRAM: A ROM-Embedded STT MRAM Cache. IEEE Electron Device Letters, 2013, 34, 1256-1258.	2.2	28
130	TraNNsformer: Neural network transformation for memristive crossbar based neuromorphic system design. , 2017, , .		28
131	In-Memory Computing in Emerging Memory Technologies for Machine Learning: An Overview. , 2020, , .		28
132	Reduction of Parametric Failures in Sub-100-nm SRAM Array Using Body Bias. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 174-183.	1.9	27
133	An Enhanced Voltage Programming Pixel Circuit for Compensating GB-Induced Variations in Poly-Si TFTs for AMOLED Displays. Journal of Display Technology, 2014, 10, 345-351.	1.3	27
134	On the energy benefits of spiking deep neural networks: A case study. , 2016, , .		27
135	Perspective: Stochastic magnetic devices for cognitive computing. Journal of Applied Physics, 2018, 123, 210901.	1.1	27
136	ABRM: Adaptive $ eta$-Ratio Modulation for Process-Tolerant Ultradynamic Voltage Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 281-290.	2.1	26
137	Ultra-Low Power Nanomagnet-Based Computing: A System-Level Perspective. IEEE Nanotechnology Magazine, 2011, 10, 778-788.	1.1	26
138	Robust Level Converter for Sub-Threshold/Super-Threshold Operation:100 mV to 2.5 V. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1429-1437.	2.1	26
139	sBSNN: Stochastic-Bits Enabled Binary Spiking Neural Network With On-Chip Learning for Energy Efficient Neuromorphic Computing at the Edge. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2546-2555.	3.5	26
140	Computing Approximately, and Efficiently. , 2015, , .		25
141	High-Density and Robust STT-MRAM Array Through Device/Circuit/Architecture Interactions. IEEE Nanotechnology Magazine, 2015, 14, 1024-1034.	1.1	25
142	Trifecta: A Nonspeculative Scheme to Exploit Common, Data-Dependent Subcritical Paths. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 53-65.	2.1	24
143	Spin-Transfer Torque Magnetic neuron for low power neuromorphic computing. , 2015, , .		24
144	Magnetic Tunnel Junction as an On-Chip Temperature Sensor. Scientific Reports, 2017, 7, 11764.	1.6	24

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145	High-Density SOT-MRAM Based on Shared Bitline Structure. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1600-1603.	2.1	24
146	Significance Driven Hybrid 8T-6T SRAM for Energy-Efficient Synaptic Storage in Artificial Neural Networks. , 2016, , .		24
147	Spin neuron for ultra low power computational hardware. , 2012, , .		23
148	SPINTASTIC: Spin-Based Stochastic Logic for Energy-Efficient Computing. , 2015, , .		23
149	Bayesian Multi-objective Hyperparameter Optimization for Accurate, Fast, and Efficient Neural Network Accelerator Design. Frontiers in Neuroscience, 2020, 14, 667.	1.4	23
150	Constructing energy-efficient mixed-precision neural networks through principal component analysis for edge intelligence. Nature Machine Intelligence, 2020, 2, 43-55.	8.3	23
151	Estimation of statistical variation in temporal NBTI degradation and its impact on lifetime circuit performance. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	22
152	Write-Optimized STT-MRAM Bit-Cells Using Asymmetrically Doped Transistors. IEEE Electron Device Letters, 2014, 35, 1100-1102.	2.2	22
153	ASLAN: Synthesis of approximate sequential circuits. , 2014, , .		22
154	Magnetic Pattern Recognition Using Injection-Locked Spin-Torque Nano-Oscillators. IEEE Transactions on Electron Devices, 2016, 63, 1674-1680.	1.6	22
155	Tri-Mode Independent Gate FinFET-Based SRAM With Pass-Gate Feedback: Technologyâ€“Circuit Co-Design for Enhanced Cell Stability. IEEE Transactions on Electron Devices, 2013, 60, 3696-3704.	1.6	21
156	Spin-Hall Magnetic Random-Access Memory With Dual Read/Write Ports for On-Chip Caches. IEEE Magnetics Letters, 2015, 6, 1-4.	0.6	21
157	Modeling and Design Space Exploration for Bit-Cells Based on Voltage-Assisted Switching of Magnetic Tunnel Junctions. IEEE Transactions on Electron Devices, 2016, 63, 3493-3500.	1.6	21
158	Area-Efficient Nonvolatile Flip-Flop Based on Spin Hall Effect. IEEE Magnetics Letters, 2018, 9, 1-4.	0.6	21
159	Profit Aware Circuit Design Under Process Variations Considering Speed Binning. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 806-815.	2.1	20
160	Slope Interconnect Effort: Gate-Interconnect Interdependent Delay Modeling for Early CMOS Circuit Simulation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 1428-1441.	3.5	20
161	Characterization of Random Process Variations Using Ultralow-Power, High-Sensitivity, Bias-Free Sub-Threshold Process Sensor. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1838-1847.	3.5	20
162	Hardware-Software Co-Design for an Analog-Digital Accelerator for Machine Learning. , 2018, , .		20

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163	FinFET SRAM: Optimizing Silicon Fin Thickness and Fin Ratio to Improve Stability at iso Area. , 2007, , .		19
164	Magnonic Spin-Transfer Torque MRAM With Low Power, High Speed, and Error-Free Switching. IEEE Transactions on Magnetics, 2012, 48, 2016-2024.	1.2	19
165	Source-Underlapped GaSbâ€“InAs TFETs With Applications to Gain Cell Embedded DRAMs. IEEE Transactions on Electron Devices, 2016, 63, 2563-2569.	1.6	19
166	Efficient embedded learning for IoT devices. , 2016, , .		19
167	MESL: Proposal for a Non-volatile Cascadable Magneto-Electric Spin Logic. Scientific Reports, 2017, 7, 39793.	1.6	19
168	Spike timing dependent plasticity based enhanced self-learning for efficient pattern recognition in spiking neural networks. , 2017, , .		19
169	Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current. Journal of Electronic Testing: Theory and Applications (JETTA), 2005, 21, 147-159.	0.9	18
170	STT-MRAMs for future universal memories: Perspective and prospective. , 2012, , .		18
171	CLIP: Circuit Level IC Protection Through Direct Injection of Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 791-803.	2.1	18
172	The Effects of Direct Source-to-Drain Tunneling and Variation in the Body Thickness on (100) and (110) Sub-10-nm Si Double-Gate Transistors. IEEE Electron Device Letters, 2015, 36, 427-429.	2.2	18
173	In-situ, In-Memory Stateful Vector Logic Operations based on Voltage Controlled Magnetic Anisotropy. Scientific Reports, 2018, 8, 5738.	1.6	18
174	Designing Energy-Efficient Intermittently Powered Systems Using Spin-Hall-Effect-Based Nonvolatile SRAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 294-307.	2.1	18
175	Mimicking Leaky-Integrate-Fire Spiking Neuron Using Automotion of Domain Walls for Energy-Efficient Brain-Inspired Computing. IEEE Transactions on Magnetics, 2019, 55, 1-7.	1.2	18
176	Circuits and Architectures for In-Memory Computing-Based Machine Learning Accelerators. IEEE Micro, 2020, 40, 8-22.	1.8	18
177	ASLAN: Synthesis of approximate sequential circuits. , 2014, , .		18
178	Optimization of Surface Orientation for High-Performance, Low-Power and Robust FinFET SRAM. , 2006, , .		17
179	Test consideration for nanometer-scale CMOS circuits. IEEE Design and Test of Computers, 2006, 23, 128-136.	1.4	17
180	On Modeling and Evaluation of Logic Circuits under Timing Variations. , 2012, , .		17

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181	Pd/IGZO/p⁺-Si Synaptic Device with Self-Graded Oxygen Concentrations for Highly Linear Weight Adjustability and Improved Energy Efficiency. ACS Applied Electronic Materials, 2020, 2, 2390-2397.	2.0	17
182	Gradual Channel Pruning While Training Using Feature Relevance Scores for Convolutional Neural Networks. IEEE Access, 2020, 8, 171924-171932.	2.6	17
183	Controlled Forgetting: Targeted Stimulation and Dopaminergic Plasticity Modulation for Unsupervised Lifelong Learning in Spiking Neural Networks. Frontiers in Neuroscience, 2020, 14, 7.	1.4	17
184	Non-adaptive and adaptive filter implementation based on sharing multiplication. , 0, , .		16
185	Oxide Thickness Optimization for Digital Subthreshold Operation. IEEE Transactions on Electron Devices, 2008, 55, 685-688.	1.6	16
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