Makoto Nagata

List of Publications by Year in Descending Order

198 papers	1,342 citations	16 h-index	27 g-index
277 ext. papers	1,705 ext. citations	1.6 avg, IF	4.34 L-index

#	Paper	IF	Citations
198	3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance. *IEEE Transactions on Electron Devices*, **2021**, 68, 2077-2082	2.9	4
197	Landside capacitor efficacy among multi-chip-module using Si-interposer. *IEICE Electronics Express*, **2021**, 18, 20210070-20210070	0.5	1
196	Diffusional Side-Channel Leakage From Unrolled Lightweight Block Ciphers: A Case Study of Power Analysis on PRINCE. *IEEE Transactions on Information Forensics and Security*, **2021**, 16, 1351-1364	8	0
195	Physical Attack Protection Techniques for IC Chip Level Hardware Security. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 1-10	2.6	2
194	Low-cost distance-spoofing attack on FMCW radar and its feasibility study on countermeasure. *Journal of Cryptographic Engineering*, **2021**, 11, 289-298	1.9	5
193	A dual-mode successive approximation register analog to digital converter to detect malicious off-chip power noise measurement attacks. *Japanese Journal of Applied Physics*, **2021**, 60, SBBL03	1.4	1
192	Design and concept proof of an inductive impulse self-destructor in sense-and-react countermeasure against physical attacks. *Japanese Journal of Applied Physics*, **2021**, 60, SBBL01	1.4	5
191	Secure Cryptographic Unit as Root-of-Trust for IoT Era. *IEICE Transactions on Electronics*, **2021**,	0.4	3
190	. *IEEE Letters on EMC Practice and Applications*, **2020**, 2, 15-20	0.5	4
189	An IC-level countermeasure against laser fault injection attack by information leakage sensing based on laser-induced opto-electric bulk current density. *Japanese Journal of Applied Physics*, **2020**, 59, SGGL02	1.4	3
188	A Random Interrupt Dithering SAR Technique for Secure ADC against Reference-Charge Side-Channel Attack **2020**,		2
187	A 0.6-V Adaptive Voltage Swing Serial Link Transmitter Using Near Threshold Body Bias Control and Jitter Estimation. *IEICE Transactions on Electronics*, **2020**, E103.C, 497-504	0.4	
186	Development of electro-copper plating with nanodiamonds for electronic interconnects in advanced packaging. *Japanese Journal of Applied Physics*, **2020**, 59, SLLD04	1.4	0
185	. *IEEE Transactions on Computers*, **2020**, 69, 534-548	2.5	5
184	. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 2747-2755	5.5	6
183	A Random Interrupt Dithering SAR Technique for Secure ADC Against Reference-Charge Side-Channel Attack. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 14-18	3.5	8
182	On-Chip Physical Attack Protection Circuits for Hardware Security : Invited Paper **2019**,		2

181	A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2019**, 9, 502-510	1.7	6
180	Side-channel leakage from sensor-based countermeasures against fault injection attack. *Microelectronics Journal*, **2019**, 90, 63-71	1.8	3
179	Power Delivery Network and Integrity in 3D-IC Chips **2019**, 41-52		
178	Evaluation of Near-Field Undesired Radio Waves from Semiconductor Switching Circuits **2019**,		2
177	A Low-Cost Replica-Based Distance-Spoofing Attack on mmWave FMCW Radar **2019**,		5
176	Evaluation of Undesired Radio Waves Below −170 dBm/Hz From Semiconductor Switching Devices for Impact on Wireless Communications. *IEEE Letters on EMC Practice and Applications*, **2019**, 1, 72-76	0.5	1
175	A Fast Side-Channel Leakage Simulation Technique Based on IC Chip Power Modeling. *IEEE Letters on EMC Practice and Applications*, **2019**, 1, 83-87	0.5	5
174	Electromagnetic Noises **2019**, 129-161		
173	Design of SRAM Resilient Against Dynamic Voltage Variations **2019**, 579-591		
172	Deployment of EMC-Compliant IC Chip Techniques in Design for Hardware Security. *Lecture Notes in Computer Science*, **2019**, 1-4	0.9	1
171	Magnetic Composite Sheets in IC Chip Packaging for Suppression of Undesired Noise Emission to Wireless Communication Channels **2019**,		2
170	In-Place Power Noise and Signal Waveform Measurements on LVDS Channels in Fan-Out Multiple IC Chip Packaging **2019**,		2
169	A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices **2019**,		1
168	A 0.72pJ/bit 400□m2 Physical Random Number Generator Utilizing SAR Technique for Secure Implementation on Sensor Nodes. *IEICE Transactions on Electronics*, **2019**, E102.C, 530-537	0.4	
167	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs **2019**,		2
166	A study on substrate noise coupling among TSVs in 3D chip stack. *IEICE Electronics Express*, **2018**, 15, 20180460-20180460	0.5	2
165	A Demonstration of a HT-Detection Method Based on Impedance Measurements of the Wiring Around ICs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1320-1324	3.5	7
164	. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 2889-2897	5.5	6

163	Supply-Chain Security Enhancement by Chaotic Wireless Chip-Package-Board Interactive PUF **2018**,		2
162	A 286 F2/Cell Distributed Bulk-Current Sensor and Secure Flush Code Eraser Against Laser Fault Injection Attack on Cryptographic Processor. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 3174-3182	5.5	15
161	Suppression of Unnecessary Radio Wave Radiated from Inverter Equipment Using Noise Suppression Sheet **2018**,		1
160	Analysis of Mixed PUF-TRNG Circuit Based on SR-Latches in FD-SOI Technology **2018**,		3
159	A 286F2/cell distributed bulk-current sensor and secure flush code eraser against laser fault injection attack **2018**,		7
158	Measurement and Analysis of Power Noise Characteristics for EMI Awareness of Power Delivery Networks in 3-D Through-Silicon Via Integration. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2018**, 8, 277-285	1.7	3
157	Design Methodology and Validity Verification for a Reactive Countermeasure Against EM Attacks. *Journal of Cryptology*, **2017**, 30, 373-391	2.1	10
156	An FPGA-compatible PLL-based sensor against fault injection attack **2017**,		4
155	Superior decoupling capacitor for three-dimensional LSI with ultrawide communication bus. *Japanese Journal of Applied Physics*, **2017**, 56, 04CC05	1.4	5
154	Protecting cryptographic integrated circuits with side-channel information. *IEICE Electronics Express* , **2017**, 14, 20162005-20162005	0.5	4
153	Analysis of patterned magnetic thin-film noise suppressor for RF IC chip **2017**,		2
152	Exploiting Bitflip Detector for Non-invasive Probing and its Application to Ineffective Fault Analysis **2017**,		1
151	Enhancing reactive countermeasure against EM attacks with low overhead **2017**,		2
150	Chaos, deterministic non-periodic flow, for chip-package-board interactive PUF **2017**,		3
149	Susceptibility evaluation of CAN transceiver circuits with in-place waveform capturing under RF DPI **2017**,		2
148	A 2.5ns-latency 0.39pJ/b 289㎟2/Gb/s ultra-light-weight PRINCE cryptographic processor **2017**,		1
147	Simulation techniques for EMC compliant design of automotive IC chips and modules **2017**,		5
146	A 500 MHz-BW -52.5 dB-THD Voltage-to-Time Converter Utilizing Two-Step Transition Inverter Delay Lines in 28 nm CMOS. *IEICE Transactions on Electronics*, **2017**, E100.C, 560-567	0.4	

145	A 500MHz-BW 52.5dB-THD Voltage-to-Time Converter utilizing a two-step transition inverter **2016**,		3
144	Ring Oscillator under Laser: Potential of PLL-based Countermeasure against Laser Fault Injection **2016**,		14
143	EMI performance of power delivery networks in 3D TSV integration **2016**,		4
142	On-chip substrate-bounce monitoring for laser-fault countermeasure **2016**,		5
141	PLL to the rescue **2016**,		18
140	Mixed-Signal Noise Coupling in System-on-Chip Design: Modeling, Analysis, and Validation **2016**, 663-688		
139	Physical authentication using side-channel information **2016**,		4
138	An Extended Direct Power Injection Method for In-Place Susceptibility Characterization of VLSI Circuits Against Electromagnetic Interference. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2347-2351	2.6	4
137	A novel methodology for testing hardware security and trust exploiting On-Chip Power noise Measurement **2015**,		4
136	In-Place Signal and Power Noise Waveform Capturing Within 3-D Chip Stacking. *IEEE Design and Test*, **2015**, 32, 87-98	1.4	9
135	EM attack sensor **2015**,		7
134	A 1 mm Pitch $80 times 80$ Channel 322 Hz Frame-Rate Multitouch Distribution Sensor With Two-Step Dual-Mode Capacitance Scan. *IEEE Journal of Solid-State Circuits*, **2015**, 50, 2741-2749	5.5	6
133	A Silicon-Level Countermeasure Against Fault Sensitivity Analysis and Its Evaluation. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1429-1438	2.6	6
132	Analysis of on-chip digital noise coupling path for wireless communication IC test chip **2015**,		1
131	Analysis of intra-chip degital noise coupling path in fully LTE compliant RF receiver test chip **2015**,		2
130	IC Chip Authentication and Guarantee. *Ieice Ess Fundamentals Review*, **2015**, 8, 177-182	0.1	2
129	Optimal error feedback filters for uniform quantizers at remote sensors **2015**,		5
128	Proactive and reactive protection circuit techniques against EM leakage and injection **2015**,		1

127	On-chip integrated magnetic thin-film solution to countermeasure digital noise on RF IC **2015**,		10
126	Side-channel leakage on silicon substrate of CMOS cryptographic chip **2014**,		8
125	A local EM-analysis attack resistant cryptographic engine with fully-digital oscillator-based tamper-access sensor **2014**,		17
124	Measurements and Analysis of Substrate Noise Coupling in TSV-Based 3-D Integrated Circuits. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, **2014**, 4, 1026-1037	1.7	16
123	Timing margin enhancement technique for current mode interface. *IEICE Electronics Express*, **2014**, 11, 20140766-20140766	0.5	1
122	Diagnosis of Signaling and Power Noise Using In-Place Waveform Capturing for 3D Chip Stacking. *IEICE Transactions on Electronics*, **2014**, E97.C, 557-565	0.4	1
121	A study on power integrity in a 3D chip stack using dynamic power supply current emulation and power noise monitoring **2014**,		2
120	An intermittent-driven supply-current equalizer for 11x and 4x power-overhead savings in CPA-resistant 128bit AES cryptographic processor **2014**,		10
119	**2014**,		1
118	12.4 A 1mm-pitch 80□0-channel 322Hz-frame-rate touch sensor with two-step dual-mode capacitance scan **2014**,		4
117	Emulation of high-frequency substrate noise generation in CMOS digital circuits. *Japanese Journal of Applied Physics*, **2014**, 53, 04EE06	1.4	2
116	Integrated-circuit countermeasures against information leakage through EM radiation **2014**,		4
115	Introduction to the Special Issue on the 2014 IEEE International Solid-State Circuits Conference (ISSCC). *IEEE Journal of Solid-State Circuits*, **2014**, 49, 2743-2747	5.5	
114	EM Attack Is Non-invasive? - Design Methodology and Validity Verification of EM Attack Sensor. *Lecture Notes in Computer Science*, **2014**, 1-16	0.9	16
113	A 40-nm Resilient Cache Memory for Dynamic Variation Tolerance Delivering 91 Failure Rate Improvement under 35% Supply Voltage Fluctuation. *IEICE Transactions on Electronics*, **2014**, E97.C, 332-341	0.4	
112	Chip Level Simulation of Substrate Noise Coupling and Interference in RF ICs with CMOS Digital Noise Emulator. *IEICE Transactions on Electronics*, **2014**, E97.C, 546-556	0.4	1
111	Power Noise Measurements of Cryptographic VLSI Circuits Regarding Side-Channel Information Leakage. *IEICE Transactions on Electronics*, **2014**, E97.C, 272-279	0.4	3
110	AC Power Supply Noise Simulation of CMOS Microprocessor with LSI Chip-Package-Board Integrated Model. *IEICE Transactions on Electronics*, **2014**, E97.C, 264-271	0.4	1

109	Measurements of SRAM sensitivity against AC power noise with effects of device variation **2013**,		3
108	Immunity evaluation of inverter chains against RF power on power delivery network **2013**,		2
107	In-system diagnosis of RF ICs for tolerance against on-chip in-band interferers **2013**,		13
106	False Operation of Static Random Access Memory Cells under Alternating Current Power Supply Voltage Variation. *Japanese Journal of Applied Physics*, **2013**, 52, 04CE14	1.4	2
105	Measurement-based diagnosis of wireless communication performance in the presence of in-band interferers in RF ICs **2013**,		1
104	Measurements and simulation of substrate noise coupling in RF ICs with CMOS digital noise emulator **2013**,		8
103	Noise analysis using on-chip waveform monitor in bandgap voltage references **2013**,		3
102	In-band spurious attenuation in LTE-class RFIC chip using a soft magnetic thin film **2013**,		2
101	A 100GB/s wide I/O with 4096b TSVs through an active silicon interposer with in-place waveform capturing **2013**,		33
100	**2013**,		1
99	Power current modeling of cryptographic VLSI circuits for analysis of side channel attacks **2013**,		2
98	Equivalent Circuit Representation of Silicon Substrate Coupling of Passive and Active RF Components. *IEICE Transactions on Electronics*, **2013**, E96.C, 875-883	0.4	1
97	A Fast Power Current Simulation of Cryptographic VLSI Circuits for Side Channel Attack Evaluation. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2013**, E96.A, 2533-2541	0.4	1
96	Design of Effective Supply Voltage Monitor for Measuring Power Rails of Integrated Circuits. *IEICE Transactions on Electronics*, **2013**, E96.C, 538-545	0.4	
95	Measurements and Simulation of Sensitivity of Differential-Pair Transistors against Substrate Voltage Variation. *IEICE Transactions on Electronics*, **2013**, E96.C, 884-893	0.4	1
94	Performance Evaluation of Probing Front-End Circuits for On-Chip Noise Monitoring. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2013**, E96.A, 2516-2523	0.4	1
93	Introduction to the Special Issue on the 2011 Symposium on VLSI Circuits. *IEEE Journal of Solid-State Circuits*, **2012**, 47, 795-796	5.5	
92	In-tier diagnosis of power domains in 3D TSV ICs **2012**,		1

91	Co-evaluation of power supply noise of CMOS microprocessor using on-board magnetic probing and on-chip waveform capturing techniques **2012**,		1
90	Monitoring effective supply voltage within power rails of integrated circuits **2012**,		2
89	Co-simulation of On-Chip and On-Board AC Power Noise of CMOS Digital Circuits. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2012**, E95.A, 2284-2291	0.4	2
88	Evaluation of SRAM-Core Susceptibility against Power Supply Voltage Variation. *IEICE Transactions on Electronics*, **2012**, E95.C, 586-593	0.4	3
87	Modeling and Analysis of Substrate Noise Coupling in Analog and RF ICs. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2012**, E95-A, 430-438	0.4	5
86	On-Chip In-Place Measurements of Vth and Signal/Substrate Response of Differential Pair Transistors. *IEICE Transactions on Electronics*, **2012**, E95-C, 137-145	0.4	
85	A fast power current analysis methodology using capacitor charging model for side channel attack evaluation **2011**,		5
84	Extraction of lumped RC elements representing substrate coupling of RF devices **2011**,		3
83	An On-Chip Waveform Capturer and Application to Diagnosis of Power Delivery in SoC Integration. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 789-796	5.5	38
82	Introduction to the Special Issue on the 2010 Symposium on VLSI Circuits. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 719-720	5.5	
81	Microprocessor power noise measurements with different levels of resource occupancy. *IEICE Electronics Express*, **2011**, 8, 182-188	0.5	
80	Evaluation of Thin Film Noise Suppressor Applied to Noise Emulator Chip Implemented in 65 nm CMOS Technology. *IEEE Transactions on Magnetics*, **2011**, 47, 4485-4488	2	6
79	A diagnosis testbench of analog IP cores against on-chip environmental disturbances **2011**,		1
78	Evaluation of substrate noise coupling in RFICs (invited) **2011**,		1
77	Accurate analysis of substrate sensitivity of active transistors in an analog circuit **2011**,		3
76	An on-chip waveform capturer for diagnosing off-chip power delivery **2011**,		2
75	On-Chip Single Tone Pseudo-Noise Generator for Analog IP Noise Tolerance Measurement. *IEICE Transactions on Electronics*, **2011**, E94-C, 1024-1031	0.4	1
74	A Continuous-Time Waveform Monitoring Technique for On-Chip Power Noise Measurements in VLSI Circuits. *IEICE Transactions on Electronics*, **2011**, E94-C, 495-503	0.4	

73	A Diagnosis Testbench of Analog IP Cores for Characterization of Substrate Coupling Strength. *IEICE Transactions on Electronics*, **2011**, E94-C, 1016-1023	0.4	
72	An on-chip waveform capturing technique pursuing minimum cost of integration **2010**,		9
71	On-chip in-situ measurements of Vth and AC gain of differential pair transistors **2010**,		2
70	Reference Complementary Metal Oxide Semiconductor Circuits and Test Structures for Evaluation of Dynamic Noise in Power Delivery Networks. *Japanese Journal of Applied Physics*, **2010**, 49, 04DE01	1.4	1
69	On-chip sine-wave noise generator for analog IP noise tolerance measurements **2010**,		5
68	On-chip waveform capture and diagnosis of power delivery in SoC integration **2010**,		8
67	Modeling of Power Noise Generation in Standard-Cell Based CMOS Digital Circuits. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2010**, E93-A, 440-447	0.4	9
66	An Arbitrary Digital Power Noise Generator Using 65 nm CMOS Technology. *IEICE Transactions on Electronics*, **2010**, E93-C, 820-826	0.4	4
65	Chip-to-Chip Half Duplex Spiking Data Communication over Power Supply Rails. *IEICE Transactions on Electronics*, **2010**, E93-C, 842-848	0.4	
64	VLSI????????????????. *Journal of Japan Institute of Electronics Packaging*, **2010**, 13, 259-262	0.1	
63	An on-chip continuous time power supply noise monitoring technique **2009**,		7
62	Evaluation of environmental noise susceptibility of RF circuits using direct power injection **2009**,		3
61	A full chip integrated power and substrate noise analysis framework for mixed-signal SoC design **2009**,		7
60	Experimental Evaluation of Dynamic Power Supply Noise and Logical Failures in Microprocessor Operations. *IEICE Transactions on Electronics*, **2009**, E92-C, 475-482	0.4	1
59	On-Chip Power Noise Measurements and Simulation Technologies of Digital LSIs. *Journal of Japan Institute of Electronics Packaging*, **2009**, 12, 581-586	0.1	1
58	Experimental evaluation of digital-circuit susceptibility to voltage variation in dynamic frequency scaling **2008**,		3
57	Measurement-Based Analysis of Electromagnetic Immunity in LSI Circuit Operation. *IEICE Transactions on Electronics*, **2008**, E91-C, 936-944	0.4	4
56	On-Die Monitoring of Substrate Coupling for Mixed-Signal Circuit Isolation. *Japanese Journal of Applied Physics*, **2007**, 46, 2244-2251	1.4	

55	Chip-Level Substrate Noise Analysis with Emphasis of Vertical Impurity Profile for Isolation **2007**,		7
54	An On-Chip Multichannel Waveform Monitor for Diagnosis of Systems-on-a-Chip Integration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2007**, 15, 1101-1110	2.6	23
53	On-Die Supply-Voltage Noise Sensor with Real-Time Sampling Mode for Low-Power Processor Applications **2007**,		7
52	Fine-Grained In-Circuit Continuous-Time Probing Technique of Dynamic Supply Variations in SoCs **2007**,		13
51	Evaluation of Isolation Structures against High-Frequency Substrate Coupling in Analog/Mixed-Signal Integrated Circuits. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2007**, E90-A, 380-387	0.4	4
50	Experimental Verification of Power Supply Noise Modeling for EMI Analysis through On-Board and On-Chip Noise Measurements. *IEICE Transactions on Electronics*, **2007**, E90-C, 1282-1290	0.4	5
49	On-Chip Measurements Complementary to Design Flow for Integrity in SoCs. *Proceedings - Design Automation Conference*, **2007**,		2
48	Chip-Level Substrate Coupling Analysis with Reference Structures for Verification. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2007**, E90-A, 2651-2660	0.4	9
47	Delay Variation Analysis in Consideration of Dynamic Power Supply Noise Waveform **2006**,		4
46	On-Chip Analog Circuit Diagnosis in Systems-on-Chip Integration **2006**,		8
45	Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation. *Proceedings of the IEEE*, **2006**, 94, 2109-2138	14.3	76
44	Simulation of integrated circuit immunity with LECCS model **2006**,		12
43	A built-in technique for probing power supply and ground noise distribution within large-scale digital integrated circuits. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 813-819	5.5	58
42	Measurements of Digital Signal Delay Variation Due to Dynamic Power Supply Noise **2005**,		7
41	A Cellular-Automaton-Type Region Extraction Algorithm and its FPGA Implementation. *Journal of Robotics and Mechatronics*, **2005**, 17, 378-386	0.7	1
40	A multinanodot floating-gate MOSFET circuit for spiking neuron models. *IEEE Nanotechnology Magazine*, **2003**, 2, 158-164	2.6	13
39	A multi-nano-dot circuit and structure using thermal-noise-assisted tunneling for stochastic associative processing. *Journal of Nanoscience and Nanotechnology*, **2002**, 2, 343-9	1.3	3
38	Physical design guides for substrate noise reduction in CMOS digital circuits. *IEEE Journal of Solid-State Circuits*, **2001**, 36, 539-549	5.5	54

37	A PWM analog memory programming circuit for floating-gate MOSFETs with 75-/spl mu/s programming time and 11-bit updating resolution. *IEEE Journal of Solid-State Circuits*, **2001**, 36, 1286-1290	5.5	12
36	A 1-D CMOS PWM Cellular Neural Network Circuit and Resistive-Fuse Network Operation **2001**,		4
35	Quantum-dot structures measuring Hamming distance for associative memories. *Superlattices and Microstructures*, **2000**, 27, 613-616	2.8	6
34	An Analog-Digital Merged Neural Circuit Using Pulse Width Modulation Technique. *Analog Integrated Circuits and Signal Processing*, **2000**, 25, 319-328	1.2	
33	Substrate Noise Simulation Techniques for Analog-Digital Mixed LSI Design. *Analog Integrated Circuits and Signal Processing*, **2000**, 25, 209-217	1.2	2
32	Substrate crosstalk analysis in mixed signal CMOS integrated circuits **2000**,		2
31	A single-electron stochastic associative processing circuit robust to random background-charge effects and its structure using nanocrystal floating-gate transistors. *Nanotechnology*, **2000**, 11, 154-160	3.4	16
30	. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2000**, 47, 1652-1657		12
29	Measurements and analyses of substrate noise waveform in mixed-signal IC environment. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2000**, 19, 671-678	2.5	44
28	A Feature Associative Processor for Image Recognition Based on a A-D Merged Architecture. *IFIP Advances in Information and Communication Technology*, **2000**, 77-88	0.5	
27	The architecture of delta sigma analog-to-digital converters using a voltage-controlled oscillator as a multibit quantizer. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **1999**, 46, 941-945		65
26	A PWM signal processing core circuit based on a switched current integration technique. *IEEE Journal of Solid-State Circuits*, **1998**, 33, 53-60	5.5	18
25	Nonlinear function generators and chaotic signal generators using a pulse-width modulation method. *Electronics Letters*, **1997**, 33, 1351	1.1	2
24	PWM signal processing architecture for intelligent systems. *Computers and Electrical Engineering*, **1997**, 23, 393-405	4.3	1
23	Photo-Electronic Crossbar Switching Network for Multiprocessor Systems **1997**, 505-510		
22	Optically Interconnected Kohonen Net for Pattern Recognition. *Japanese Journal of Applied Physics*, **1996**, 35, 1405-1409	1.4	7
21	A concept of analog-digital merged circuit architecture for future VLSIC. *Analog Integrated Circuits and Signal Processing*, **1996**, 11, 83	1.2	12
20	Magnetic field dependence of the device-width-dependent breakdown current in the quantum Hall effect. *Surface Science*, **1994**, 305, 161-165	1.8	12

19	Breakdown of the Quantum Hall Effect in GaAs/AlGaAs Heterostructures Due to Current. *Journal of the Physical Society of Japan*, **1994**, 63, 2303-2313	1.5	68
18	Device-width dependence of plateau width in quantum Hall states. *Physica B: Condensed Matter*, **1993**, 184, 17-20	2.8	33
17	A minimum-distance search circuit using dual-line PWM signal processing and charge-packet counting techniques		8
16	An on-chip multi-channel waveform monitor for mixed-signal VLSI diagnostics		1
15	Substrate-noise and random-fluctuations reduction with self-adjusted forward body bias		11
14	On-chip multi-channel waveform monitoring for diagnostics of mixed-signal VLSI circuits		3
13	An integrated timing and dynamic supply noise verification for nano-meter CMOS SoC designs		8
12	Equivalent circuit modeling of guard ring structures for evaluation of substrate crosstalk isolation		1
11	A built-in technique for probing power-supply noise distribution within large-scale digital integrated circuits		2
10	A design of transponder IC for highly collision resistive RFID systems		5
9	Dynamic power-supply and well noise measurement and analysis for high frequency body-biased circuits		15
8	Isolation strategy against substrate coupling in CMOS mixed-signal/RF circuits		14
7	Modeling substrate noise generation in CMOS digital integrated circuits		8
6	A cellular-automaton-type image extraction algorithm and its implementation using an FPGA		2
5	Quantitative characterization of substrate noise for physical design guides in digital circuits		3
4	Effects of power-supply parasitic components on substrate noise generation in large-scale digital circuits		8
3	Chip-level substrate noise analysis with network reduction by fundamental matrix computation		4
2	Measurements and analyses of substrate noise waveform in mixed signal IC environment		6

List of Publications

1 Low resistive ultra shallow junction for sub 0.1 /spl mu/m MOSFETs formed by Sb implantation 3