

# Gabor

## List of Publications by Year in descending order

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citing authors

#	ARTICLE	IF	CITATIONS
1	Switched-Capacitor Integrator with Slew-Rate Enhancement and Low Distortion. , 2021, , .	0	
2	Noise-Shaping SAR ADC Using a Two-Capacitor Digitally Calibrated DAC With 82.6-dB SNDR and 90.9-dB SFDR. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4001-4012.	5.4	6
3	A Charge-Domain Switched-G <sub>m</sub> -C Band-Pass Filter Using Interleaved Semi-Passive Charge-Sharing Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 600-610.	5.4	4
4	Pseudo-Pseudo-Differential Multibit Delta-Sigma Modulator. , 2020, , .	1	
5	Noise-Shaping SAR ADC Using a Two-Capacitor Digitally Calibrated DAC with 85.1 dB DR and 91 dB SFDR. , 2020, , .	3	
6	Incremental Delta-Sigma ADCs: A Tutorial Review. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 4161-4173.	5.4	40
7	Slewing Mitigation Technique for Switched Capacitor Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 3251-3261.	5.4	6
8	Efficient Calibration of Feedback DAC in Delta Sigma Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 826-830.	3.0	6
9	Digital Correction of DAC Nonlinearity in Multi-Bit Feedback A/D Converters: Invited tutorial. , 2020, , .	4	
10	Thoughts on Engineering Creativity [Point of View]. Proceedings of the IEEE, 2019, 107, 1223-1226.	21.3	0
11	An Amplifier-Free 2 SAR-VCO MASH ADC. , 2019, , .	0	
12	Predictive Noise Shaping SAR ADC. , 2019, , .	2	
13	An 11-Bit 250-nW 10-kS/s SAR ADC With Doubled Input Range for Biomedical Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 61-73.	5.4	46
14	A 13b-ENOB Noise Shaping SAR ADC with a Two-Capacitor DAC. , 2018, , .	10	
15	Single-Loop Delta-Sigma ADC Using Noise-Coupled VCO Quantizer. , 2018, , .	1	
16	A two-capacitor SAR-assisted multi-step incremental ADC with a single amplifier achieving 96.6 dB SNDR over 1.2 kHz BW. , 2017, , .	10	
17	Pseudo-pseudo-differential circuits. , 2017, , .	7	
18	Passive 3rdorder delta-sigma ADC with VCO-based quantizer. , 2017, , .	3	

#	ARTICLE	IF	CITATIONS
19	Power-on digital calibration method for delta-Sigma ADCs. , 2016, , .		4
20	A noise-coupled time-interleaved delta-sigma modulator with shifted loop delays. , 2015, , .		3
21	Two-stage &#x0394;&#x03A3; ADC with noise-coupled VCO-based quantizer. , 2015, , .		2
22	A passive CMOS low-pass filter for high speed and high SNDR applications. , 2015, , .		5
23	Low-power duty-cycle tuned filters. , 2014, , .		0
24	Sequential interstage correlated double sampling: A switched-capacitor technique for high accuracy systems. , 2014, , .		1
25	Bootstrapping techniques for floating switches in switched-capacitor circuits. , 2014, , .		3
26	A noise-coupled low-distortion delta-sigma ADC with shifted loop delays. , 2014, , .		1
27	A fully-differential input amplifier with band-pass filter for biosensors. , 2014, , .		7
28	Multi-step counting ADC. , 2014, , .		1
29	Multi-channel mixed-signal noise source with applications to stochastic equalization. , 2012, , .		0
30	Digital foreground calibration methods for SAR ADCs. , 2012, , .		6
31	Calibration technique for SAR analog-to-digital converters. , 2012, , .		1
32	Calibration technique for SAR analog-to-digital converters. Analog Integrated Circuits and Signal Processing, 2012, 73, 301-309.	1.4	2
33	A semi-synchronous SAR ADC. Analog Integrated Circuits and Signal Processing, 2012, 71, 407-410.	1.4	3
34	A 75dB SNDR, 10MHz conversion bandwidth stage-shared 2-2 MASH &#x0394;&#x03A3; modulator dissipating 9mW. , 2011, , .		5
35	Hybrid delta-sigma ADC. Analog Integrated Circuits and Signal Processing, 2010, 63, 293-298.	1.4	0
36	Radix-based digital correction technique for two-capacitor DACs. , 2010, , .		2

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37	An op-amp sharing technique for continuous-time &#x0394;&#x03A3; modulators. , 2010, , .	1	
38	Design techniques for discrete-time delta-sigma ADCs with extra loop delay. , 2010, , .	4	
39	Switched-resistor tuning technique for highly linear G<inf>m</inf>-C filter design. , 2010, , .	0	
40	Low-power switched-capacitor integrator for delta-sigma ADCs. , 2010, , .	0	
41	A new zero-optimization scheme for noise-coupled &#x0394;&#x03A3; ADCs. , 2010, , .	2	
42	Noise-coupled low-power incremental ADCs. , 2010, , .	2	
43	Micropower Data Converters: A Tutorial. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 405-410.	3.0	9
44	Low Distortion &#x0394;&#x03A3; Modulator Employing modified charge-pump based switched-capacitor integrator. , 2010, , .	2	
45	&#x0394;&#x03A3; ADCs with second-order noise-shaping enhancement. , 2009, , .	6	
46	Low-distortion double-sampling &#x0394;&#x03A3; ADC using a direct-charge-transfer adder. , 2009, , .	3	
47	An enhanced dual-path &#x0394;&#x03A3; analog-to-digital converter. , 2009, , .	0	
48	Improved low-distortion &#x0394;&#x03A3; ADC topology. , 2009, , .	4	
49	Wideband &#x0394;&#x03A3; ADCs using direct-charge-transfer adder. , 2009, , .	4	
50	Double-sampled &#x0394;&#x03A3; modulator with relaxed feedback timing. , 2009, , .	0	
51	Noise-coupled continuous-time &#x0394;&#x03A3; ADCs. , 2009, , .	1	
52	A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC. IEEE Journal of Solid-State Circuits, 2008, 43, 1195-1206.	5.4	56
53	New architectures for low-power delta-sigma analog-to-digital converter. , 2008, , .	4	
54	Efficient fully-floating double-sampling integrator for Î”Î£ ADCs. , 2008, , .	2	

#	ARTICLE	IF	CITATIONS
55	A 2.5MHz BW and 78dB SNDR delta-sigma modulator using dynamically biased amplifiers. , 2008,,.	7	
56	A Segmented Data-Weighted-Averaging Technique. , 2007,,.	10	
57	Predictive Switched-Capacitor Track-and-Hold Amplifier with Improved Linearity. , 2007,,.	0	
58	Noise-Coupled Multi-Cell Delta-Sigma ADCs. , 2007,,.	13	
59	Efficient pipelined ADCs using integer gain MDACs. , 2007,,.	1	
60	A 100-dB gain-corrected delta-sigma audio DAC with headphone driver. Analog Integrated Circuits and Signal Processing, 2007, 51, 27-31.	1.4	2
61	A New Approach to Reducing Output Ripple in Switched-Capacitor-Based Step-Down DC&ndash;DC Converters. IEEE Transactions on Power Electronics, 2006, 21, 1548-1555.	7.9	52
62	Incremental Delta-Sigma Structures for DC Measurement: an Overview. , 2006,,.	24	
63	Enhanced split-architecture delta-sigma ADC. , 2006,,.	6	
64	Multicell Delta-Sigma Data Converters. Midwest Symposium on Circuits and Systems, 2006,,.	1.0	0
65	Switched-capacitor track-and-hold amplifier with low sensitivity to op-amp imperfections. Analog Integrated Circuits and Signal Processing, 2006, 48, 267-270.	1.4	4