# Sneh Saurabh

List of Publications by Year
in descending order



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|---|---|---|---|
| 25 papers | 955 citations | 1040056 9 h-index | 888059 17 g-index |
| 26 all docs | 26 docs citations | 26 times ranked | 577 citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Novel attributes of a dual pocket tunnel field-effect transistor. Japanese Journal of Applied Physics, 2022, 61, 035001. | 1.5 | 0 |
| 2 | Modeling Multiple-Input Switching in Timing Analysis Using Machine Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 723-734. | 2.7 | 4 |
| 3 | An Efficient Timing Model of Flip-Flops Based on Artificial Neural Network. , 2021, , . | | 1 |
| 4 | Implementing a Ternary Inverter Using Dual-Pocket Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2021, 68, 5305-5310. | 3.0 | 5 |
| 5 | Effect of Drain Induced Barrier Enhancement on Subthreshold Swing and OFF-State Current of Short Channel MOSFETs: A TCAD Study. IEEE Access, 2021, 9, 141321-141328. | 4.2 | 1 |
| 6 | Drain Induced Barrier Widening and Reverse Short Channel Effects in Tunneling FETs: Investigation and Analysis. IEEE Access, 2021, 9, 150366-150372. | 4.2 | 2 |
| 7 | Reducing Breakdown Voltage in a Bipolar Impact Ionization MOSFET (BI-MOS) using Gateâ€“Source Underlap. , 2021, , . | | 0 |
| 8 | Resistive Random Access Memory: A Review of Device Challenges. IETE Technical Review (Institution of) Tj ETQq0 0 0 rgBT /Overlock 10 | 3.2 | 56 |
| 9 | Exploiting Within-Channel Tunneling in a Nanoscale Tunnel Field-Effect Transistor. IEEE Open Journal of Nanotechnology, 2020, 1, 100-108. | 2.0 | 8 |
| 10 | Realizing XOR and XNOR Functions Using Tunnel Field-Effect Transistors. IEEE Journal of the Electron Devices Society, 2020, 8, 1001-1009. | 2.1 | 7 |
| 11 | Suppression of Ambipolar current in Tunnel Field-Effect Transistor using Field-Plate. , 2020, , . | | 4 |
| 12 | Implementation of Boolean Functions Using Tunnel Field-Effect Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 146-154. | 1.5 | 7 |
| 13 | Realizing Boolean Functions Using Probabilistic Spin Logic (PSL). , 2019, , . | | 0 |
| 14 | Dopingless 1T DRAM: Proposal, Design, and Analysis. IEEE Access, 2019, 7, 88960-88969. | 4.2 | 11 |
| 15 | Implementing Logic Functions Using Independently-Controlled Gate in Double-Gate Tunnel FETs: Investigation and Analysis. IEEE Access, 2019, 7, 117591-117599. | 4.2 | 17 |
| 16 | Improving the Scalability of SOI-Based Tunnel FETs Using Ground Plane in Buried Oxide. IEEE Journal of the Electron Devices Society, 2019, 7, 435-443. | 2.1 | 26 |
| 17 | Application of Probabilistic Spin Logic (PSL) in Detecting Satisfiability of a Boolean Function. , 2019, , . | | 2 |
| 18 | Timing Closure Problem: Review of Challenges at Advanced Process Nodes and Solutions. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2019, 36, 580-593. | 3.2 | 6 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Realizing Logic Functions Using Single Double-Gate Tunnel FETs: A Simulation Study. IEEE Electron Device Letters, 2018, 39, 773-776. | 3.9 | 24 |
| 20 | Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis. Superlattices and Microstructures, 2018, 113, 261-270. | 3.1 | 68 |
| 21 | A Practical Methodology to Compress Technology Libraries Using Recursive Polynomial Representation. , 2018, , . | | 5 |
| 22 | Assessing the Impact of Temperature and Supply Voltage Variations in Near-threshold Circuits using an Analytical Model. , 2018, , . | | 0 |
| 23 | Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2011, 58, 404-410. | 3.0 | 392 |
| 24 | Estimation and Compensation of Process-Induced Variations in Nanoscale Tunnel Field-Effect Transistors for Improved Reliability. IEEE Transactions on Device and Materials Reliability, 2010, 10, 390-395. | 2.0 | 64 |
| 25 | Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis. Japanese Journal of Applied Physics, 2009, 48, 064503. | 1.5 | 124 |