

# Sneh Saurabh

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/2675824/publications.pdf>

Version: 2024-02-01

25  
papers

955  
citations

1040056

9  
h-index

888059

17  
g-index

26  
all docs

26  
docs citations

26  
times ranked

577  
citing authors

#	ARTICLE	IF	CITATIONS
1	Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2011, 58, 404-410.	3.0	392
2	Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor: Theoretical Investigation and Analysis. Japanese Journal of Applied Physics, 2009, 48, 064503.	1.5	124
3	Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis. Superlattices and Microstructures, 2018, 113, 261-270.	3.1	68
4	Estimation and Compensation of Process-Induced Variations in Nanoscale Tunnel Field-Effect Transistors for Improved Reliability. IEEE Transactions on Device and Materials Reliability, 2010, 10, 390-395.	2.0	64
5	Resistive Random Access Memory: A Review of Device Challenges. IETE Technical Review (Institution of Tj ETQq1 1,0,784314 rgBT /Ove	3.2	56
6	Improving the Scalability of SOI-Based Tunnel FETs Using Ground Plane in Buried Oxide. IEEE Journal of the Electron Devices Society, 2019, 7, 435-443.	2.1	26
7	Realizing Logic Functions Using Single Double-Gate Tunnel FETs: A Simulation Study. IEEE Electron Device Letters, 2018, 39, 773-776.	3.9	24
8	Implementing Logic Functions Using Independently-Controlled Gate in Double-Gate Tunnel FETs: Investigation and Analysis. IEEE Access, 2019, 7, 117591-117599.	4.2	17
9	Dopingless 1T DRAM: Proposal, Design, and Analysis. IEEE Access, 2019, 7, 88960-88969.	4.2	11
10	Exploiting Within-Channel Tunneling in a Nanoscale Tunnel Field-Effect Transistor. IEEE Open Journal of Nanotechnology, 2020, 1, 100-108.	2.0	8
11	Realizing XOR and XNOR Functions Using Tunnel Field-Effect Transistors. IEEE Journal of the Electron Devices Society, 2020, 8, 1001-1009.	2.1	7
12	Implementation of Boolean Functions Using Tunnel Field-Effect Transistors. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2020, 6, 146-154.	1.5	7
13	Timing Closure Problem: Review of Challenges at Advanced Process Nodes and Solutions. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2019, 36, 580-593.	3.2	6
14	A Practical Methodology to Compress Technology Libraries Using Recursive Polynomial Representation. , 2018, , .		5
15	Implementing a Ternary Inverter Using Dual-Pocket Tunnel Field-Effect Transistors. IEEE Transactions on Electron Devices, 2021, 68, 5305-5310.	3.0	5
16	Suppression of Ambipolar current in Tunnel Field-Effect Transistor using Field-Plate. , 2020, , .		4
17	Modeling Multiple-Input Switching in Timing Analysis Using Machine Learning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 723-734.	2.7	4
18	Application of Probabilistic Spin Logic (PSL) in Detecting Satisfiability of a Boolean Function. , 2019, , .		2

#	ARTICLE	IF	CITATIONS
19	Drain Induced Barrier Widening and Reverse Short Channel Effects in Tunneling FETs: Investigation and Analysis. IEEE Access, 2021, 9, 150366-150372.	4.2	2
20	An Efficient Timing Model of Flip-Flops Based on Artificial Neural Network. , 2021, , .		1
21	Effect of Drain Induced Barrier Enhancement on Subthreshold Swing and OFF-State Current of Short Channel MOSFETs: A TCAD Study. IEEE Access, 2021, 9, 141321-141328.	4.2	1
22	Realizing Boolean Functions Using Probabilistic Spin Logic (PSL). , 2019, , .		0
23	Assessing the Impact of Temperature and Supply Voltage Variations in Near-threshold Circuits using an Analytical Model. , 2018, , .		0
24	Novel attributes of a dual pocket tunnel field-effect transistor. Japanese Journal of Applied Physics, 2022, 61, 035001.	1.5	0
25	Reducing Breakdown Voltage in a Bipolar Impact Ionization MOSFET (BI-MOS) using Gate-Source Underlap. , 2021, , .		0