Yao-Wen Chang

List of Publications by Year
in descending order

276	5,338	185998 28	223531 46
papers	citations	h-index	g-index

280	280	280	976
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	High-Correlation 3D Routability Estimation for Congestion-guided Global Routing. , 2022, , .		4
2	Mixed-Cell-Height Detailed Placement Considering Complex Minimum-Implant-Area Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2128-2141.	1.9	9
3	Analytical Placement Considering the Electron-Beam Fogging Effect. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 560-573.	1.9	4
4	A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 533-546.	1.9	11
5	Timing-Driven Placement for FPGAs with Heterogeneous Architectures and Clock Constraints. , 2021, , .		3
6	A Bridge-based Compression Algorithm for Topological Quantum Circuits. , 2021, , .		3
7	VLSI Structure-aware Placement for Convolutional Neural Network Accelerator Units. , 2021, , .		4
8	Simultaneous Pre- and Free-assignment Routing for Multiple Redistribution Layers with Irregular Vias. , 2021, , .		3
9	On-chip Optical Routing with Waveguide Matching Constraints. , 2021, , .		0
10	Mixed-Cell-Height Legalization Considering Technology and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5128-5141.	1.9	9
11	Intelligent design automation for 2.5/3D heterogeneous SoC integration. , 2020, , .		2
12	DSA-Compliant Routing for 2-D Patterns Using Block Copolymer Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 267-280.	1.9	0
13	A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing. , 2019, , .		8
14	BiG. , 2019, , .		6
15	MDP-trees. , 2019, , .		6
16	Provably Good Maxâ€“Min- m -Neighbor-TSP-Based Subfield Scheduling for Electron-Beam Photomask Fabrication. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 378-391.	2.1	2
17	NTUplace4dr: A Detailed-Routing-Driven Placer for Mixed-Size Circuit Designs With Technology and Region Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 669-681.	1.9	37
18	A multithreaded initial detailed routing algorithm considering global routing guides. , 2018, , .		19

#	ARTICLE	IF	CITATIONS
19	Mixed-cell-height placement considering drain-to-drain abutment. , 2018, , .		10
20	Analytical solution of Poisson's equation and its application to VLSI global placement. , 2018, , .		10
21	Mixed-cell-height legalization considering technology and region constraints. , 2018, , .		12
22	Novel proximal group ADMM for placement considering fogging and proximity effects. , 2018, , .		7
23	Mixed-cell-height placement with complex minimum-implant-area constraints. , 2018, , .		16
24	Generalized Augmented Lagrangian and Its Applications to VLSI Global Placement. , 2018, , .		3
25	WB-trees. , 2018, , .		5
26	Efficient multi-layer obstacle-avoiding region-to-region rectilinear steiner tree construction. , 2018, , .		4
27	Generalized augmented lagrangian and its applications to VLSI global placement. , 2018, , .		6
28	DSA-friendly detailed routing considering double patterning and DSA template assignments. , 2018, , .		1
29	Nanowire-Aware Routing Considering High Cut Mask Complexity. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 964-977.	1.9	1
30	Detailed Placement for Two-Dimensional Directed Self-Assembly Technology. , 2017, , .		3
31	Fogging Effect Aware Placement in Electron Beam Lithography. , 2017, , .		7
32	Blockage-aware terminal propagation for placement wirelength minimization. , 2017, , .		0
33	Cut Redistribution With Directed-Self-Assembly Templates for Advanced 1-D Gridded Layouts. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2066-2079.	1.9	0
34	An integrated-spreading-based macro-refining algorithm for large-scale mixed-size circuit designs. , 2017, , .		3
35	Graph-Based Logic Bit Slicing for Datapath-Aware Placement. , 2017, , .		5
36	Redistribution layer routing for integrated fan-out wafer-level chip-scale packages. , 2016, , .		12

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37	DSA-compliant routing for two-dimensional patterns using block copolymer lithography. , 2016, , .		4
38	Minimum-implant-area-aware detailed placement with spacing constraints. , 2016, , .		19
39	QB-trees. , 2016, , .		9
40	Timing-driven cell placement optimization for early slack histogram compression. , 2016, , .		5
41	VCR. , 2016, , .		4
42	Circular-contour-based obstacle-aware macro placement. , 2016, , .		12
43	Overlay-Aware Detailed Routing for Self-Aligned Double Patterning Lithography Using the Cut Process. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1519-1531.	1.9	6
44	Fast Lithographic Mask Optimization Considering Process Variation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1345-1357.	1.9	38
45	Simultaneous EUV Flare Variation Minimization and CMP Control by Coupling-Aware Dummification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 598-610.	1.9	5
46	Cut redistribution with directed self-assembly templates for advanced 1-D gridded layouts. , 2016, , .		10
47	Layout-Dependent Effects-Aware Analytical Analog Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1243-1254.	1.9	42
48	Double-Patterning Aware DSA Template Guided Cut Redistribution for Advanced 1-D Gridded Designs. , 2016, , .		16
49	Detailed-routability-driven analytical placement for mixed-size designs with technology and region constraints. , 2015, , .		13
50	Provably good max-min-m-neighbor-TSP-based subfield scheduling for electron-beam photomask fabrication. , 2015, , .		1
51	Layout decomposition for Spacer-is-Metal (SIM) self-aligned double patterning. , 2015, , .		4
52	Coupling-Aware Length-Ratio-Matching Routing for Capacitor Arrays in Analog Integrated Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 161-172.	1.9	10
53	EUV and e-beam manufacturability. , 2015, , .		12
54	Stitch-Aware Routing for Multiple E-Beam Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 471-482.	1.9	5

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55	Non-stitch triple patterning-aware routing based on conflict graph pre-coloring. , 2015, , .		5
56	Layout-dependent-effects-aware analytical analog placement. , 2015, , .		12
57	Nanowire-aware routing considering high cut mask complexity. , 2015, , .		11
58	Cutting structure-aware analog placement based on self-aligned double patterning with e-beam lithography. , 2015, , .		1
59	Detailed-Routing-Driven analytical standard-cell placement. , 2015, , .		15
60	Routing-architecture-aware analytical placement for heterogeneous FPGAs. , 2015, , .		17
61	NTUplace4h: A Novel Routability-Driven Placement Algorithm for Hierarchical Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1914-1927.	1.9	59
62	Simultaneous EUV Flare Variation Minimization and CMP Control with Coupling-Aware Dummification. , 2014, , .		4
63	Simultaneous EUV flare variation minimization and CMP control with coupling-aware dummification. , 2014, , .		0
64	Fast lithographic mask optimization considering process variation. , 2014, , .		7
65	Efficient and effective packing and analytical placement for large-scale heterogeneous FPGAs. , 2014, , .		17
66	Simultaneous EUV flare- and CMP-aware placement. , 2014, , .		4
67	Routability-Driven Blockage-Aware Macro Placement. , 2014, , .		21
68	Overlay-Aware Detailed Routing for Self-Aligned Double Patterning Lithography Using the Cut Process. , 2014, , .		24
69	Buffered clock tree synthesis considering self-heating effects. , 2014, , .		1
70	Functional ECO Using Metal-Configurable Gate-Array Spare Cells. , 2014, , .		1
71	Obstacle-Avoiding Free-Assignment Routing for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 224-236.	1.9	7
72	A New Asynchronous Pipeline Template for Power and Performance Optimization. , 2014, , .		7

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73	Nonuniform Multilevel Analog Routing With Matching Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 1942-1954.	1.9	20
74	A Novel Layout Decomposition Algorithm for Triple Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2014, 33, 397-408.	1.9	50
75	Coupling-aware length-ratio-matching routing for capacitor arrays in analog integrated circuits. , 2013, , .		7
76	Layer minimization in escape routing for staggered-pin-array PCBs. , 2013, , .		2
77	ECO Optimization Using Metal-Configurable Gate-Array Spare Cells. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1722-1733.	1.9	3
78	Escape Routing for Staggered-Pin-Array PCBs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1347-1356.	1.9	10
79	TSV-Aware Analytical Placement for 3-D IC Designs Based on a Novel Weighted-Average Wirelength Model. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 497-509.	1.9	67
80	An efficient and effective analytical placer for FPGAs. , 2013, , .		39
81	Symmetrical buffered clock-tree synthesis with supply-voltage alignment. , 2013, , .		1
82	Simultaneous analog placement and routing with current flow and current density considerations. , 2013, , .		24
83	Routability-driven placement for hierarchical mixed-size circuit designs. , 2013, , .		29
84	Stitch-aware routing for multiple e-beam lithography. , 2013, , .		7
85	Multiple chip planning for chip-interposer codesign. , 2013, , .		23
86	Simultaneous OPC- and CMP-aware routing based on accurate closed-form modeling. , 2013, , .		2
87	Double patterning lithography-aware analog placement. , 2013, , .		7
88	Circuit placement challenges. Communications of the ACM, 2013, 56, 104-104.	3.3	2
89	Graph-Based Subfield Scheduling for Electron-Beam Photomask Fabrication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 189-201.	1.9	8
90	Timing ECO optimization using metal-configurable gate-array spare cells. , 2012, , .		4

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91	Obstacle-avoiding free-assignment routing for flip-chip designs. , 2012, , .		4
92	Structure-aware placement for datapath-intensive circuit designs. , 2012, , .		31
93	Non-uniform multilevel analog routing with matching constraints. , 2012, , .		25
94	Graph-based subfield scheduling for electron-beam photomask fabrication. , 2012, , .		3
95	A chip-package-board co-design methodology. , 2012, , .		5
96	A novel layout decomposition algorithm for triple patterning lithography. , 2012, , .		50
97	Simultaneous flare level and flare variation minimization with dummification in EUVL. , 2012, , .		14
98	TRECO: Dynamic Technology Remapping for Timing Engineering Change Orders. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1723-1733.	1.9	11
99	Unified Analytical Global Placement for Large-Scale Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1366-1378.	1.9	21
100	An Efficient Pre-Assignment Routing Algorithm for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 878-889.	1.9	10
101	Timing ECO Optimization Via BÃ©zier Curve Smoothing and Fixability Identification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1857-1866.	1.9	11
102	Fast Timing-Model Independent Buffered Clock-Tree Synthesis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 1393-1404.	1.9	12
103	Native-Conflict and Stitch-Aware Wire Perturbation for Double Patterning Technology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 703-716.	1.9	19
104	Escape routing for staggered-pin-array PCBs. , 2011, , .		7
105	A corner stitching compliant B[∗]-tree representation and its applications to analog placement. , 2011, , .		8
106	A SAT-based routing algorithm for cross-referencing biochips. , 2011, , .		6
107	Heterogeneous B[∗]-trees for analog placement with symmetry and regularity considerations. , 2011, , .		3
108	An EOS-Free PNP-enhanced cascoded NMOSFET structure for high voltage application. , 2011, , .		0

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109	PRICE: Power reduction by placement and clock-network co-synthesis for pulsed-latch designs. , 2011, , .		4
110	Simultaneous Layout Migration and Decomposition for Double Patterning Technology. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 284-294.	1.9	18
111	Thermal-Driven Analog Placement Considering Device Matching. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 325-336.	1.9	26
112	Cross-Contamination Aware Design Methodology for Pin-Constrained Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 817-828.	1.9	51
113	Voltage-Drop Aware Analytical Placement by Global Power Spreading for Mixed-Size Circuit Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1649-1662.	1.9	4
114	Pulsed-Latch Aware Placement for Timing-Integrity Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1856-1869.	1.9	2
115	Routability-driven analytical placement for mixed-size circuit designs. , 2011, , .		33
116	Simultaneous functional and timing ECO. , 2011, , .		18
117	TSV-aware analytical placement for 3D IC designs. , 2011, , .		74
118	Timing ECO optimization via Bézier curve smoothing and fixability identification. , 2011, , .		1
119	Hierarchical Placement with Layout Constraints. , 2011, , 61-94.		3
120	Cross-contamination aware design methodology for pin-constrained digital microfluidic biochips. , 2010, , .		20
121	Fast timing-model independent buffered clock-tree synthesis. , 2010, , .		20
122	Pulsed-latch aware placement for timing-integrity optimization. , 2010, , .		24
123	Native-conflict-aware wire perturbation for double patterning technology. , 2010, , .		17
124	Template-mask design methodology for double patterning technology. , 2010, , .		2
125	Unified analytical global placement for large-scale mixed-size circuit designs. , 2010, , .		4
126	TRECO: Dynamic technology remapping for timing Engineering Change Orders. , 2010, , .		11

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127	High variation-tolerant obstacle-avoiding clock mesh synthesis with symmetrical driving trees. , 2010, , .		11
128	Redundant-wires-aware ECO timing and mask cost optimization. , 2010, , .		10
129	Recent research development in flip-chip routing. , 2010, , .		12
130	Three-dimensional integrated circuits (3D IC) Floorplan and Power/Ground Network Co-synthesis. , 2010, , .		41
131	Design-hierarchy aware mixed-size placement for routability optimization. , 2010, , .		19
132	Blockage-avoiding buffered clock-tree synthesis for clock latency-range and skew minimization. , 2010, , .		1
133	Predictive Formulae for OPC With Applications to Lithography-Friendly Routing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 40-50.	1.9	12
134	ECO Timing Optimization Using Spare Cells and Technology Remapping. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 697-710.	1.9	24
135	Multilayer Global Routing With Via and Wire Capacity Considerations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 685-696.	1.9	22
136	Area-I/O Flip-Chip Routing for Chip-Package Co-Design Considering Signal Skews. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 711-721.	1.9	31
137	ILP-Based Pin-Count Aware Design Methodology for Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1315-1327.	1.9	31
138	Efficient provably good OPC modeling and its applications to interconnect optimization. , 2010, , .		2
139	Density gradient minimization with coupling-constrained dummy fill for CMP control. , 2010, , .		19
140	Floorplanning. , 2009, , 575-634.		5
141	High-performance global routing with fast overflow reduction. , 2009, , .		38
142	T-trees. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-28.	1.9	6
143	ILP-based pin-count aware design methodology for microfluidic biochips. , 2009, , .		29
144	Flip-chip routing with unified area-I/O pad assignments for package-board co-design. , 2009, , .		41

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145	Global and detailed routing. , 2009, , 687-749.		22
146	Thermal-driven analog placement considering device matching. , 2009, , .		25
147	Routing for manufacturability and reliability. IEEE Circuits and Systems Magazine, 2009, 9, 20-31.	2.6	8
148	A Novel Hot-Electron Programming Method in a Buried Diffusion Bit-Line SONOS Memory by Utilizing Nonequilibrium Charge Transport. IEEE Electron Device Letters, 2009, 30, 165-167.	2.2	0
149	An Integer-Linear-Programming-Based Routing Algorithm for Flip-Chip Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 98-110.	1.9	42
150	A Novel Wire-Density-Driven Full-Chip Routing System for CMP Variation Control. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 193-206.	1.9	24
151	Voltage-Island Partitioning and Floorplanning Under Timing Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 690-702.	1.9	13
152	Analog Placement Based on Symmetry-Island Formulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 791-804.	1.9	75
153	A Progressive-ILP-Based Routing Algorithm for the Synthesis of Cross-Referencing Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1295-1306.	1.9	7
154	Essential Issues in Analytical Placement Algorithms. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 145-166.	0.5	35
155	Post-floorplanning power/ground ring synthesis for multiple-supply-voltage designs. , 2009, , .		9
156	Simultaneous layout migration and decomposition for double patterning technology. , 2009, , .		28
157	Voltage-drop aware analytical placement by global power spreading for mixed-size circuit designs. , 2009, , .		5
158	Routing for chip-package-board co-design considering differential pairs. , 2008, , .		2
159	Predictive formulae for OPC with applications to lithography-friendly routing. , 2008, , .		19
160	A New Multilevel Framework for Large-Scale Interconnect-Driven Floorplanning. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 286-294.	1.9	29
161	Multilayer Obstacle-Avoiding Rectilinear Steiner Tree Construction Based on Spanning Graphs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2007-2016.	1.9	22
162	BioRoute: A Network-Flow-Based Routing Algorithm for the Synthesis of Digital Microfluidic Biochips. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1928-1941.	1.9	101

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163	Metal-Density-Driven Placement for CMP Variation and Routability. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 2145-2155.	1.9	12
164	Obstacle-Avoiding Rectilinear Steiner Tree Construction Based on Spanning Graphs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 643-653.	1.9	60
165	Full-Chip Routing Considering Double-Via Insertion. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 844-857.	1.9	61
166	Effective Wire Models for X-Architecture Placement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 654-658.	1.9	3
167	NTUplace3: An Analytical Placer for Large-Scale Mixed-Size Designs With Preplaced Blocks and Density Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1228-1240.	1.9	260
168	An Optimal Network-Flow-Based Simultaneous Diode and Jumper Insertion Algorithm for Antenna Fixing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1055-1065.	1.9	8
169	MP-Trees: A Packing-Based Macro Placement Algorithm for Modern Mixed-Size Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1621-1634.	1.9	37
170	Area-I/O flip-chip routing for chip-package co-design. , 2008, , .		5
171	Sensitivity-based multiple-Vt cell swapping for leakage power reduction. , 2008, , .		1
172	Constraint graph-based macro placement for modern mixed-size circuit designs. , 2008, , .		3
173	Routability-driven analytical placement by net overlapping removal for large-scale mixed-size designs. , 2008, , .		41
174	A progressive-ILP based routing algorithm for cross-referencing biochips. , 2008, , .		63
175	Metal-density driven placement for cmp variation and routability. , 2008, , .		6
176	Multi-layer global routing considering via and wire capacities. , 2008, , .		0
177	Temporal floorplanning using the three-dimensional transitive closure subGraph. ACM Transactions on Design Automation of Electronic Systems, 2007, 12, 37.	1.9	20
178	Placement of defect-tolerant digital microfluidic biochips using the T-tree formulation. ACM Journal on Emerging Technologies in Computing Systems, 2007, 3, 13.	1.8	86
179	Post-placement leakage optimization for partially dynamically reconfigurable FPGAs. , 2007, , .		6
180	Statistical circuit optimization considering device andinterconnect process variations. , 2007, , .		3

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181	X-architecture placement based on effective wire models. , 2007, , .		1
182	Efficient obstacle-avoiding rectilinear steiner tree construction. , 2007, , .		39
183	MP-trees. Proceedings - Design Automation Conference, 2007, , .	0.0	14
184	Challenges and Solutions in Modern VLSI Placement. , 2007, , .		5
185	Novel wire density driven full-chip routing for CMP variation control. , 2007, , .		4
186	Recent Research and Emerging Challenges in Physical Design for Manufacturability/Reliability. , 2007, , .		10
187	A Network-Flow-Based RDL Routing Algorithmz for Flip-Chip Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1417-1429.	1.9	74
188	MB^{ast}-Tree: A Multilevel Floorplanner for Large-Scale Building-Module Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1430-1444.	1.9	2
189	Power/Ground Network and Floorplan Cosynthesis for Fast Design Convergence. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 693-704.	1.9	17
190	An Exact Jumper-Insertion Algorithm for Antenna Violation Avoidance/Fixing Considering Routing Obstacles. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 719-733.	1.9	5
191	Multilevel Full-Chip Routing With Testability and Yield Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1625-1636.	1.9	10
192	An Optimal Jumper-Insertion Algorithm for Antenna Avoidance/Fixing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1818-1829.	1.9	8
193	ECO timing optimization using spare cells. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	5
194	Multilevel Full-Chip Gridless Routing With Applications to Optical-Proximity Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1041-1053.	1.9	18
195	BioRoute: a network-flow based routing algorithm for digital microfluidic biochips. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	2
196	An efficient algorithm for statistical circuit optimization using lagrangian relaxation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	0
197	Efficient multi-layer obstacle-avoiding rectilinear steiner tree construction. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3
198	An Integer Linear Programming Based Routing Algorithm for Flip-Chip Design. Proceedings - Design Automation Conference, 2007, , .	0.0	18

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199	NTUplace3: An Analytical Placer for Large-Scale Mixed-Size Designs. Integrated Circuits and Systems, 2007, , 289-309.	0.2	0
200	Novel full-chip gridless routing considering double-via insertion. , 2006, , .		29
201	Voltage Island Aware Floorplanning for Power and Timing Optimization. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	10
202	Current Path Analysis for Electrostatic Discharge Protection. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	0
203	A High-Quality Mixed-Size Analytical Placer Considering Preplaced Blocks and Density Constraints. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6
204	Modern floorplanning based on B/sup */-tree and fast simulated annealing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 637-650.	1.9	104
205	Multilevel routing with jumper insertion for antenna avoidance. The Integration VLSI Journal, 2006, 39, 420-432.	1.3	5
206	An optimal jumper insertion algorithm for antenna avoidance/fixing on general routing trees with obstacles. , 2006, , .		11
207	Simultaneous block and I/O buffer floorplanning for flip-chip design. , 2006, , .		14
208	Placement of digital microfluidic biochips using the t-tree formulation. , 2006, , .		44
209	A high-quality mixed-size analytical placer considering preplaced blocks and density constraints. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	56
210	A novel framework for multilevel full-chip gridless routing. , 2006, , .		17
211	Charge-based capacitance measurement for bias-dependent capacitance. IEEE Electron Device Letters, 2006, 27, 390-392.	2.2	40
212	Novel full-chip gridless routing considering double-via insertion. Proceedings - Design Automation Conference, 2006, , .	0.0	5
213	Thermal-Driven Interconnect Optimization by Simultaneous Gate and Wire Sizing. , 2006, , .		0
214	An Optimal Simultaneous Diode/Jumper Insertion Algorithm for Antenna Fixing. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	0
215	Modern floorplanning based on fast simulated annealing. , 2005, , .		61
216	Multilevel full-chip routing for the X-based architecture. , 2005, , .		32

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