Tian-Sheuan Chang

List of Publications by Year
in descending order

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		393982	329751
134	2,072	19	37
papers	citations	h-index	g-index

135	135	135	1304
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	RangeSeg: Range-Aware Real Time Segmentation of 3D LiDAR Point Clouds. IEEE Transactions on Intelligent Vehicles, 2022, 7, 93-101.	9.4	31
2	Device quantization policy in variation-aware in-memory computing design. Scientific Reports, 2022, 12, 112.	1.6	6
3	Sparse Compressed Spiking Neural Network Accelerator for Object Detection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 2060-2069.	3.5	11
4	A Real-Time 1280 Ã— 720 Object Detection Chip With 585 MB/s Memory Traffic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 816-825.	2.1	2
5	Hardware-Robust In-RRAM-Computing for Object Detection. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 547-556.	2.7	2
6	An 1-bit by 1-bit High Parallelism In-RRAM Macro with Co-Training Mechanism for DCNN Applications. , 2022, , .		1
7	A 14 Î¼J/Decision Keyword-Spotting Accelerator With In-SRAMComputing and On-Chip Learning for Customization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1184-1192.	2.1	3
8	IMU Based Deep Stride Length Estimation With Self-Supervised Learning. IEEE Sensors Journal, 2021, 21, 7380-7387.	2.4	9
9	VSA: Reconfigurable Vectorwise Spiking Neural Network Accelerator. , 2021, , .		6
10	Pre-RTL DNN Hardware Evaluator With Fused Layer Support. , 2021, , .		1
11	Determining motions with an IMU during level walking and slope and stair walking. Journal of Sports Sciences, 2020, 38, 62-69.	1.0	19
12	VWA: Hardware Efficient Vectorwise Accelerator for Convolutional Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 145-154.	3.5	31
13	Image Synthesis With Efficient Defocus Blur for Stereoscopic Displays. IEEE Access, 2020, 8, 176304-176312.	2.6	0
14	Real-Time Wearable Gait Phase Segmentation for Running And Walking. , 2020, , .		8
15	Zebra: Memory Bandwidth Reduction for CNN Accelerators with Zero Block Regularization of Activation Maps. , 2020, , .		1
16	Efficient Accelerator for Dilated and Transposed Convolution with Decomposition. , 2020, , .		14
17	A Secure File Sharing System Based on IPFS and Blockchain. , 2020, , .		28
18	Real Time On Sensor Gait Phase Detection with 0.5KB Deep Learning Model. , 2020, , .		0

#	Article	IF	Citations
19	VSCNN: Convolution Neural Network Accelerator with Vector Sparsity. , 2019, , .		6
20	Run Time Adaptive Network Slimming for Mobile Environments. , 2019, , .		0
21	NV-BNN. , 2019, , .		20
22	Sub-nA Low-Current HZO Ferroelectric Tunnel Junction for High-Performance and Accurate Deep Learning Acceleration. , 2019, , .		34
23	Deep Gait Tracking With Inertial Measurement Unit. , 2019, 3, 1-4.		3
24	Data and Hardware Efficient Design for Convolutional Neural Network. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1642-1651.	3.5	45
25	Mitigating Asymmetric Nonlinear Weight Update Effects in Hardware Neural Network Based on Analog Resistive Synapse. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 116-124.	2.7	87
26	Fast rate distortion optimization with adaptive context group modeling for HEVC. , 2017, , .		2
27	Challenges and opportunities toward online training acceleration using RRAM-based hardware neural network. , 2017, , .		26
28	Perceptual oriented depth cue enhancement for stereoscopic view synthesis. , 2016, , .		0
29	Fast intra prediction algorithm and design for high efficiency video coding. , 2016, , .		15
30	A QFHD 30-frames/s HEVC Decoder Design. IEEE Transactions on Circuits and Systems for Video Technology, 2016, 26, 724-735.	5.6	11
31	A multi-bin constant throughput CABAC decoder for HEVC. , 2015, , .		0
32	Fast Motion Estimation Algorithm and Design for Real Time QFHD High Efficiency Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2015, 25, 1533-1544.	5.6	54
33	Fast rate distortion optimization design for HEVC intra coding. , 2015, , .		4
34	Low complexity real time BCI for stroke rehabilitation. , 2015, , .		3
35	A hardware-efficient deblocking filter design for HEVC. , 2015, , .		7
36	Thermal-aware memory management unit of 3D-stacked DRAM for 3D high definition (HD) video. , 2014, , .		2

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37	Analysis and implementation of lowâ€power perceptual multiband noise reduction for the hearing aids application. IET Circuits, Devices and Systems, 2014, 8, 516-525.	0.9	7
38	Correction to â€œLow Complexity Formant Estimation Adaptive Feedback Cancellation for Hearing Aids Using Pitch Based Processingâ€•[Aug 14 1248-1259]. IEEE/ACM Transactions on Audio Speech and Language Processing, 2014, 22, 2256-2256.	4.0	0
39	Bare Finger 3D Air-Touch System Using an Embedded Optical Sensor Array for Mobile Displays. Journal of Display Technology, 2014, 10, 13-18.	1.3	19
40	A real time 1080P 30FPS Gaussian Mixture Modeling design for background subtraction and object extraction. , 2014, , .		1
41	Gradient-based PU size selection for HEVC intra prediction. , 2014, , .		15
42	Low Complexity Formant Estimation Adaptive Feedback Cancellation for Hearing Aids Using Pitch Based Processing. IEEE/ACM Transactions on Audio Speech and Language Processing, 2014, 22, 1248-1259.	4.0	19
43	135-MHz 258-K Gates VLSI Design for All-Intra H.264/AVC Scalable Video Encoder. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 636-647.	2.1	5
44	Algorithm and Architecture Design of Bandwidth-Oriented Motion Estimation for Real-Time Mobile Video Applications. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 33-42.	2.1	7
45	Fast zero block detection and early CU termination for HEVC Video Coding. , 2013, , .		3
46	Three-Dimensional Virtual Touch Display System for Multi-User Applications. Journal of Display Technology, 2013, 9, 921-928.	1.3	9
47	Bare finger 3D airâ€touch system with embedded multiwavelength optical sensor arrays for mobile 3D displays. Journal of the Society for Information Display, 2013, 21, 381-388.	0.8	5
48	Fast prediction unit selection for HEVC fractional pel motion estimation design. , 2013, , .		4
49	Stereo Matching and Viewpoint Synthesis FPGA Implementation. , 2013, , 69-106.		6
50	Fast SIFT Design for Real-Time Visual Feature Extraction. IEEE Transactions on Image Processing, 2013, 22, 3158-3167.	6.0	150
51	An Efficient Mode Preselection Algorithm for Fractional Motion Estimation in H.264/AVC Scalable Video Extension. IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23, 1837-1848.	5.6	1
52	A reconfigurable inverse transform architecture design for HEVC decoder. , 2013, , .		16
53	A high throughput CAVLC design for HEVC. , 2012, , .		0
54	A low complexity speech coder for binaural communication in hearing aids. , 2012, , .		1

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55	Fast intra prediction algorithm with transform domain edge detection for HEVC. , 2012, , .		6
56	Sub muW Noise Reduction for CIC Hearing Aids. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 937-947.	2.1	2
57	Fast disparity estimation for 3DTV applications. , 2012, , .		0
58	A Highly Efficient VLSI Architecture for H.264/AVC Level 5.1 CABAC Decoder. IEEE Transactions on Circuits and Systems for Video Technology, 2012, 22, 272-281.	5.6	13
59	A low-power body-channel communication system for binaural hearing aids. , 2012, , .		1
60	A 135 MHz 542 k Gates High Throughput H.264/AVC Scalable High Profile Decoder. IEEE Transactions on Circuits and Systems for Video Technology, 2012, 22, 626-635.	5.6	2
61	A 385 MHz 13.54 K Gates Delay Balanced Two-Level CAVLC Decoder for Ultra HD H.264/AVC Video. IEEE Transactions on Circuits and Systems for Video Technology, 2012, 22, 1604-1610.	5.6	2
62	A lossless embedded compression codec engine for HD video decoding. , 2012, , .		4
63	VLSI Architecture for Real-Time HD1080p View Synthesis Engine. IEEE Transactions on Circuits and Systems for Video Technology, 2011, 21, 1329-1340.	5.6	29
64	A 94fps view synthesis engine for HD1080p video. , 2011, , .		6
65	Bandwidth-constrained motion estimation for real-time mobile video application. , 2011, , .		0
66	A 124 Mpixels/s VLSI Design for Histogram-Based Joint Bilateral Filtering. IEEE Transactions on Image Processing, 2011, 20, 3231-3241.	6.0	24
67	Real-time high-definition stereo matching on FPGA. , 2011, , .		62
68	Fast algorithm for local stereo matching in disparity estimation. , 2011, , .		1
69	An efficient mode pre-selection algorithm for H.264/AVC scalable video extension fractional motion estimation. , 2011, , .		1
70	Efficient inter-layer prediction hardware design with extended spatial scalability for H.264/AVC scalable extension. , 2010, , .		0
71	Stereoscopic images generation with directional Gaussian filter. , 2010, , .		28
72	Fast stereo matching with predictive search range. , 2010, , .		2

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73	Low memory cost bilateral filtering using stripe-based sliding integral histogram. , 2010, , .		7
74	A high throughput VLSI design with hybrid memory architecture for H.264/AVC CABAC decoder. , 2010, , .		4
75	Algorithm and Architecture of Disparity Estimation With Mini-Census Adaptive Support Weight. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 792-805.	5.6	105
76	Architecture Design of Belief Propagation for Real-Time Disparity Estimation. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1555-1564.	5.6	7
77	Perceptual multiband spectral subtraction for noise reduction in hearing aids. , 2010, , .		7
78	RD Optimized Bandwidth Efficient Motion Estimation and Its Hardware Design With On-Demand Data Access. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1565-1576.	5.6	3
79	A low-power Mandarin-specific hearing aid chip. , 2010, , .		4
80	A memory efficient Fine Grain Scalability coefficient encoding method for H.264/AVC Scalable Video Extension. , 2009, , .		0
81	Low-memory cost belief propagation architecture for disparity estimation. , 2009, , .		0
82	Bandwidth-rate-distortion optimized motion estimation. , 2009, , .		0
83	A 140-MHz 94 K Gates HD1080p 30-Frames/s Intra-Only Profile H.264 Encoder. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 432-436.	5.6	52
84	Memory analysis for H.264/AVC scalable extension encoder. , 2009, , .		1
85	A Hardware-Efficient H.264/AVC Motion-Estimation Design for High-Definition Video. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 1526-1535.	3.5	54
86	Hardware Efficient Skip Mode Detection for H.264/AVC. , 2008, , .		3
87	Architecture Design of Shape-Adaptive Discrete Cosine Transform and Its Inverse for MPEG-4 Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2008, 18, 375-386.	5.6	9
88	Adaptive De-Interlacing With Robust Overlapped Block Motion Compensation. IEEE Transactions on Circuits and Systems for Video Technology, 2008, 18, 1437-1440.	5.6	3
89	Analysis of color space and similarity measure impact on stereo block matching. , 2008, , .		6
90	A 242mW 10mm² 1080p H.264/AVC High-Profile Encoder Chip. , 2008, , .		20

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91	Data reuse analysis of local stereo matching. , 2008, , .		2
92	ISID : In-order scan and indexed diffusion segmentation algorithm for stereo vision. , 2008, , .		0
93	Block-based belief propagation with in-place message updating for stereo vision. , 2008, , .		1
94	A Low Cost Context Adaptive Arithmetic Coder for H.264/MPEG-4 AVC Video Coding. , 2007, , .		14
95	PMRME: A Parallel Multi-Resolution Motion Estimation Algorithm and Architecture for HDTV Sized H.264 Video Coding. , 2007, , .		17
96	SIFME: A Single Iteration Fractional-Pel Motion Estimation Algorithm and Architecture for HDTV Sized H.264 Video Coding. , 2007, , .		15
97	A 61MHz 72K Gates 1280Ã—720 30FPS H.264 Intra Encoder. , 2007, , .		8
98	A Fast Algorithm and Its VLSI Architecture for Fractional Motion Estimation for H.264/MPEG-4 AVC Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2007, 17, 578-583.	5.6	52
99	Low Memory Cost Block-Based Belief Propagation for Stereo Correspondence. , 2007, , .		20
100	Optimal Data Mapping for Motion Compensation in H.264 Video Decoding. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	9
101	An in-place architecture for the deblocking filter in H.264/AVC. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 530-534.	2.3	46
102	High Performance Context Adaptive Variable Length Coding Encoder for MPEG-4 AVC/H.264 Video Coding. , 2006, , .		6
103	Combined Frame Memory Motion Compensation for Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 1280-1285.	5.6	4
104	A Display Order Oriented Scalable Video Decoder. , 2006, , .		0
105	A Memory Bandwidth Optimized Interpolator for Motion Compensation in the H.264 Video Decoding. , 2006, , .		5
106	A Fast Algorithm and Its Architecture for Motion Estimation in MPEG-4 AVC/H.264 Video Coding. , 2006, , .		7
107	SoC Memory System Design. , 2006, , 73-118.		6
108	A memory-efficient realization of cyclic convolution and its application to discrete cosine transform. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 445-453.	5.6	39

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109	Fast block type decision algorithm for intra prediction in H.264 FRext. , 2005, , .		26
110	On the data reuse and memory bandwidth analysis for full-search block-matching VLSI architecture. IEEE Transactions on Circuits and Systems for Video Technology, 2002, 12, 61-72.	5.6	246
111	Hardware-efficient DFT designs with cyclic convolution and subexpression sharing. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 886-892.	2.3	28
112	Low-power FIR filter realization with differential coefficients and inputs. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 137-145.	2.3	26
113	A simple processor core design for DCT/IDCT. IEEE Transactions on Circuits and Systems for Video Technology, 2000, 10, 439-447.	5.6	66
114	A new RSA cryptosystem hardware design based on Montgomery's algorithm. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 1998, 45, 908-913.	2.3	77
115	A Multiplierless Reconfigurable Resizer For Multi-window Image Display. , 1997, , .		0
116	A multiplierless reconfigurable resizer for multi-window image display. IEEE Transactions on Consumer Electronics, 1997, 43, 826-832.	3.0	0
117	Embedded memory module design for video signal processing. , 0, , .		1
118	The IDCT processor on the adder-based distributed arithmetic. , 0, , .		4
119	The IC design of a high speed RSA processor. , 0, , .		5
120	Low power FIR filter realization with differential coefficients and input. , 0, , .		2
121	Hardware efficient transform designs with cyclic formulation and subexpression sharing. , 0, , .		4
122	A compact IDCT processor for HDTV applications. , 0, , .		1
123	Platform-dependent database and performance estimation for video application in embedded system. , 0, , .		1
124	An MPEG-4 shape-adaptive inverse DCT with zero skipping and auto-aligned transpose memory. , 0, , .		1
125	A low power and memory efficient distributed arithmetic design and its DCT application. , 0, , .		1
126	Combined Frame Memory Architecture for Motion Compensation in Video Decoding. , 0, , .		1

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127	Fast Three Step Intra Prediction Algorithm for 4x4 blocks in H.264. , 0, , .		58
128	Architecture design of MPEG-4 texture decoder supporting object-based video coding. , 0, , .		0
129	Fast motion estimation by adaptive early termination. , 0, , .		4
130	A bandwidth efficient subsampling-based block matching architecture for motion estimation. , 0, , .		0
131	A fast fractional pel motion estimation algorithm for H.264/MPEG-4 AVC. , 0, , .		11
132	A 1280Ã—720 Pixels 3OFrames/s H.264/MPEG-4 AVC Intra Encoder. , 0, , .		7
133	A zero-skipping multi-symbol CAVLC decoder for MPEG-4 AVC/H.264. , 0, , .		23
134	Low-Complexity Stereo Matching and Viewpoint Interpolation in Embedded Consumer Applications. , 0, , 307-330.		0